2N3442

High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

Features

- Collector −Emitter Sustaining Voltage − $V_{CEO(sus)}$ = 140 Vdc (Min)
- Excellent Second Breakdown Capability
- Pb−Free Package is Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CB}	160	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current − Continuous − Peak	I_C	10 15	Adc
Base Current − Continuous − Peak	I_B	7.0 −	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C (Note 2)	P_D	117 0.67	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.17	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.
2. This data guaranteed in addition to JEDEC registered data.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

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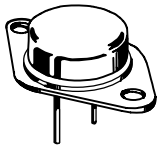
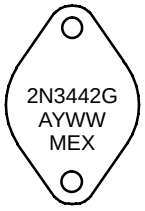
10 AMPERE
POWER TRANSISTOR
NPN SILICON
140 VOLTS − 117 WATTS



TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM



2N3442 = Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
2N3442	TO−204	100 Units / Tray
2N3442G	TO−204 (Pb−Free)	100 Units / Tray

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	−	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	−	200	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 − −	 5.0 30	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 7.5	 70 −	−
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	−	5.0	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	5.7	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 4) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	f_T	80	−	kHz
Small−Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	12	72	−

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
4. $f_T = |h_{fe}| \bullet f_{test}$

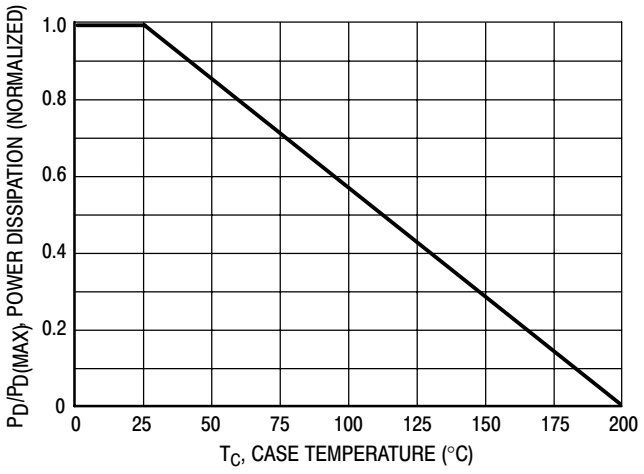


Figure 1. Power Derating

ACTIVE REGION SAFE OPERATING AREA INFORMATION

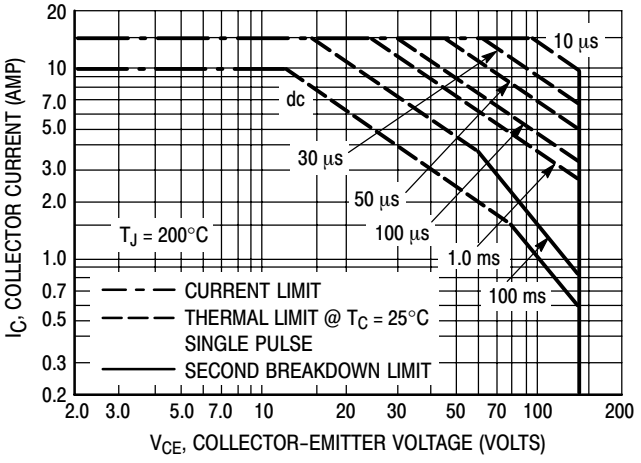


Figure 2. 2N3442

There are two limitations on the power−handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

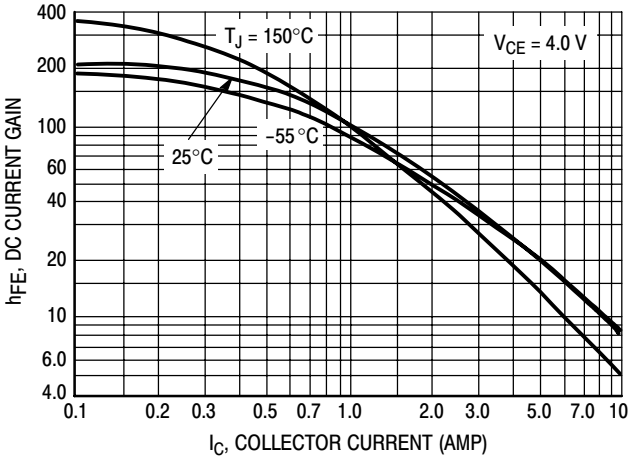


Figure 3. DC Current Gain

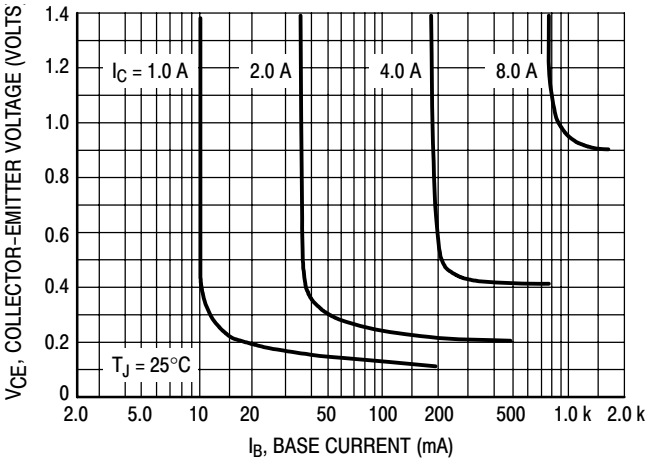
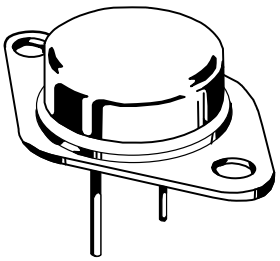


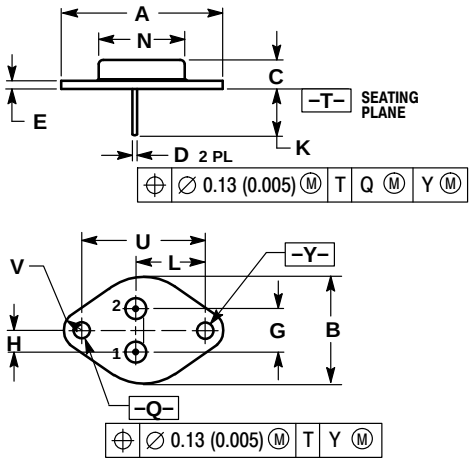
Figure 4. Collector−Saturation Region



SCALE 1:1

TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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