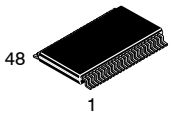
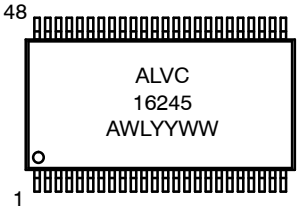
Low-Voltage 16-Bit Bidirectional Transceiver with 3.6 V Tolerant Inputs and Outputs

74ALVC16245



TSSOP48 12.5x6.1
CASE 948BQ

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

General Description

The ALVC16245 contains sixteen non−inverting bidirectional buffers with 3−STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3−STATE control inputs which can be shorted together for full 16−bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 74ALVC16245 is designed for low voltage (1.65 V to 3.6 V) V_{CC} applications with I/O capability up to 3.6 V.

The 74ALVC16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65 V – 3.6 V V_{CC} Supply Operation
- 3.6 V Tolerant Inputs and Outputs
- t_{PD}
  - 3.0 ns max for 3.0 V to 3.6 V V_{CC}
  - 3.5 ns max for 2.3 V to 2.7 V V_{CC}
  - 6.0 ns max for 1.65 V to 1.95 V V_{CC}
- Power−down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal*
- Uses Patented Noise/EMI Reduction Circuitry
- Latch−up conforms to JEDEC JED78
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

*To ensure the high−impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull−up resistor; the minimum value of the resistor is determined by the current−sourcing capability of the driver.

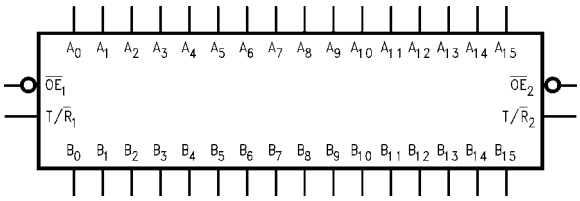


Figure 1. Logic Symbol

Connection Diagram

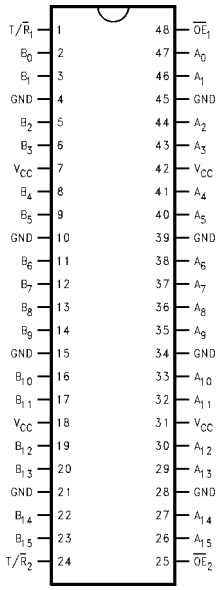


Figure 2. Pin Assignment of TSSOP

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs of 3–STATE Outputs
B_0–B_{15}	Side B Inputs of 3–STATE Outputs
NC	No Connect

TRUTH TABLE

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
Z = High Impedance

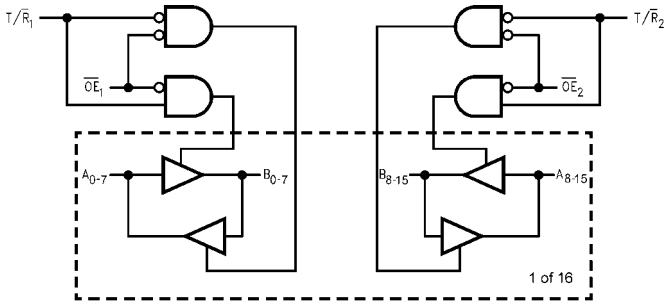


Figure 3. Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +4.6	V
DC Input Voltage	V_I	−0.5 to +4.6	V
Output Voltage (Note 1)	V_O	−0.5 to V_{CC} + 0.5	V
DC Input Diode Current, V_I < 0 V	I_{IK}	−50	mA
DC Output Diode Current, V_O < 0 V	I_{OK}	−50	mA
DC Output Source/Sink Current	I_{OH}/I_{OL}	±50	mA
DC V_{CC} or GND Current per Supply Pin	I_{CC} or GND	±100	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O Absolute Maximum Rating must be observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Operating Voltage	1.65	3.6	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Free Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8 V to 2.0 V, V_{CC} = 3.0 V	0	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. Floating or unused control inputs must be held HIGH or LOW.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 – 1.95 2.3 – 2.7 2.7 – 3.6	0.65 x V_{CC} 1.7 2.0		V
V_{IL}	LOW Level Input Voltage		1.65 – 1.95 2.3 – 2.7 2.7 – 3.6		0.35 x V_{CC} 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	1.65 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3 2.7 3.0	1.7 2.2 2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	1.65 – 3.6		0.2	V
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 12 mA	2.3 2.7		0.7 0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6 V	3.6		±5.0	μA
I_{OZ}	3−STATE Output Leakage	0 ≤ V_O ≤ 3.6 V	3.6		±10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} – 0.6 V	3 – 3.6		750	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$								Units
		$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3$ V ±0.3 V		$V_{CC} = 2.7$ V		$V_{CC} = 2.5$ V ±0.2 V		$V_{CC} = 1.8$ V ±0.15 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	1.3	3	1.5	3.5	1.0	3.0	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.3	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns

CAPACITANCE

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0$ V or V_{CC}	3.3	6	pF
C_{IO}	Input, Output Capacitance		$V_O = 0$ V or V_{CC}	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, $C_L = 50$ pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms

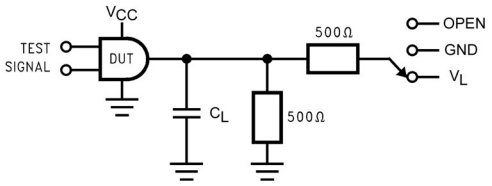


Figure 4. AC Test Circuit

Values for Figure 4

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

VARIABLE MATRIX

(Input Characteristics: f = 1 MHz; $t_r = t_f$ = 2 ns; Z_0 = 50 Ω)

Symbol	V_{CC}			
	3.3 V ±0.3 V	**2.7 V**	**2.5 V ±0.2 V**	**1.8 V ±0.15 V**
V_{mi}	1.5 V	1.5 V	V_{CC} / 2	V_{CC} / 2
V_{mo}	1.5 V	1.5 V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V
V_L	6 V	6 V	V_{CC} * 2	V_{CC} * 2

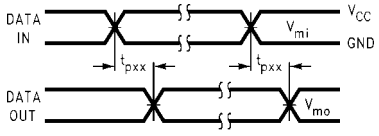


Figure 5. Waveform for Inverting and Non−Inverting Functions

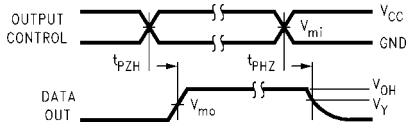


Figure 6. 3−STATE Output High Enable and Disable Times for Low Voltage Logic

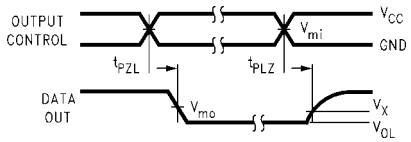


Figure 7. 3−STATE Output Low Enable and Disable Times for Low Voltage Logic

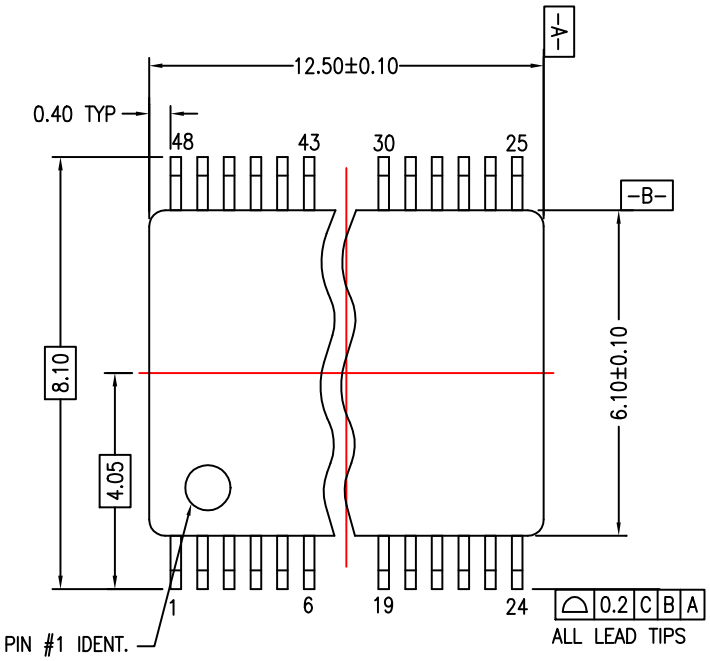
ORDERING INFORMATION

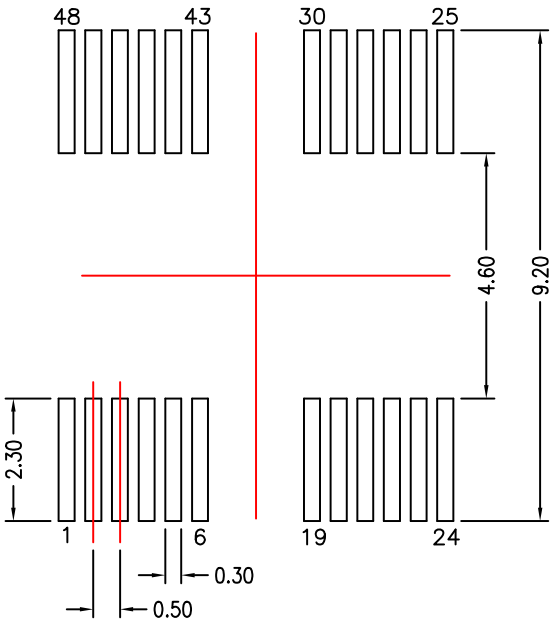
Device	Package	Shipping†
74ALVC16245MTDX	TSSOP48 12.5x6.1 (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

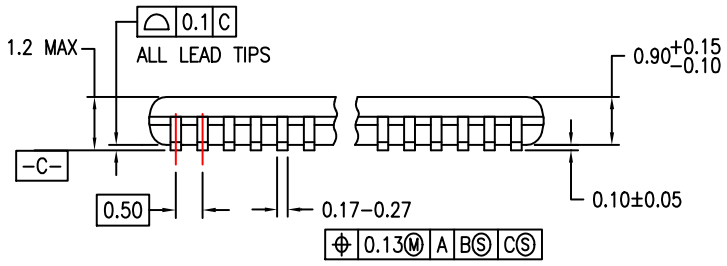
TSSOP48 12.5x6.1
CASE 948BQ
ISSUE O

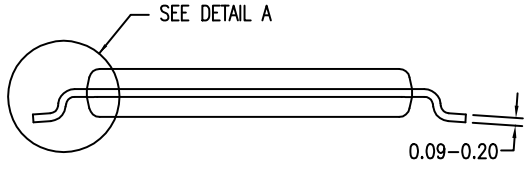
DATE 30 SEP 2016

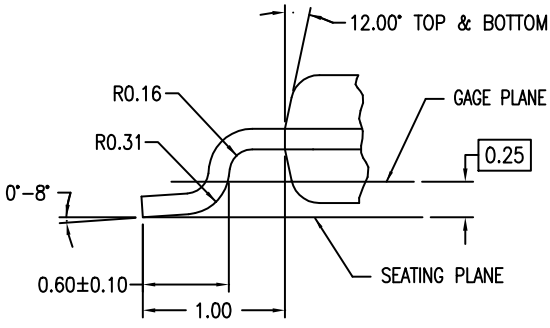




LAND PATTERN RECOMMENDATION







DETAIL A

DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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DESCRIPTION:	**TSSOP48 12.5X6.1**	**PAGE 1 OF 1**

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