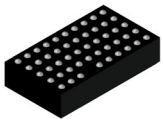
Audio Processor for Digital Hearing Aids

EZAIRO 8310 Hybrid



SIP49
CASE 127FH

Introduction

Ezairo® 8310 is an open−programmable DSP−based hybrid specifically designed for use in high−performance hearing aids and hearables. The Ezairo 8310 hybrid includes the Ezairo 8300 System−on−Chip (SoC), **onsemi**'s high−end DSP processor, as well as the LE25S161 **onsemi**'s ultra−low power flash memory.

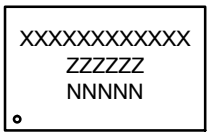
Ezairo 8300 includes six programmable or semi−programmable processing cores, providing a high degree of parallelism and flexibility:

- The CFX is an open−programmable dual−Harvard 24 bits digital signal processor (DSP) providing support for any type of audio signal processing
- The ArmR CortexR−M3 processor is a 32−bit RISC processor providing support for general processing and interfacing to external components
- The HEAR configurable accelerator core is optimized for pre−programmed functions that are frequently needed in audio signal processing
- The Filter Engine allows time domain filtering and supports an ultra−low−delay audio path
- The LPDSP32 is an open−programmable dual−Harvard 32−bit DSP
- The Neural Network Accelerator that allows the Ezairo 8300 to perform neural network computations in a highly efficient and flexible way.

Ezairo 8300 includes 4 ADCs with signal detection mode and two direct digital output drivers, with high quality and ultra−low power performances. Ezairo 8300 also includes peripherals and interfaces needed to make it a complete hardware platform when combined with the LE25S161 flash memory.

Ezairo 8300 also includes a Neural Network Accelerator that allows the Ezairo 8300 to perform neural network computations is a highly efficient and flexible way.

MARKING DIAGRAM



XXXX = Specific Device Code
ZZZ = Assembly Lot Code
NNN = Serial Number

ORDERING INFORMATION

Device	Package	Shipping
E8310−0−101A49−AG	SIP49 (RoHS compliant)	250 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

KEY FEATURES

- **High Performance:** Best in class MIPS/mW.
- **Programmable Flexibility:** the open−programmable DSP−based system can be customized to the specific signal processing needs of manufacturers. Algorithms and features can be modified or completely new concepts implemented without having to modify the chip.
- **Highly−integrated SoC:** the six−core architecture includes a CFX DSP, an Arm Cortex−M3 Processor, a HEAR Configurable Accelerator, a programmable Filter Engine, a LPDSP 32 DSP and a Neural Network Accelerator. The system also includes an efficient input/output controller (IOC), system memories, input and output stages along with a full complement of peripherals and interfaces.
- **CFX DSP:** a highly cycle−efficient, programmable core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. The CFX can be used as the master of the whole Ezairo 8300 SoC.
- **Arm Cortex−M3 Processor:** a complete subsystem that can be used as the master of the whole Ezairo 8300 SoC.
- **HEAR Configurable Accelerator:** a highly optimized signal processing engine designed to perform common signal processing operations and complex standard filterbanks.
- **Programmable Filter Engine:** a filtering system that allows applying a various range of pre− or post−processing filtering, such as IIR, FIR and biquad filters.
- **LPDSP32:** a highly cycle−efficient, programmable core that uses a 32−bit fixed−point, dual−MAC, dual−Harvard architecture.
- **Neural Network Accelerator (NNA)**: a configurable hardware accelerator dedicated to support neural networks with high energy efficiency.
- **Selectable System Clock Speeds:** from 2.56 MHz up to 61.44 MHz, with clock throttling capabilities to optimize the computing performance versus power consumption ratio.
- **Adaptive Voltage Scaling:** automatically adjusts the digital supply voltage (VDDC) level using a critical path speed measurement block. This feature allows to optimize the SoC's power consumption in all situations.
- **Ultra−low Delay path:** the programmable Filter Engine supports an ultra−low−delay audio path of min 10.4 μs (analog input to analog output) for features such as active noise cancellation.
- **Ultra−low Power Consumption:** <0.7 mA @ 15.24 MHz system clock (CFX 97%, Arm Cortex−M3 processor 40%, HEAR 77%, FENG 9%, 2 ADC @ 20 kHz, 1 OD, 1 LSAD).
- **High fidelity audio system:** 108 dB system dynamic range, up to 64 KHz of sampling frequency.
- **Output drivers:** capable of driving multiple types of speakers.
- **Versatile Memory Architecture:** a total of 1433 kB of memory, shared between the six programmable or semi−programmable cores.
- **Data Security:** sensitive program data can be encrypted for storage in external NVM to prevent unauthorized parties from gaining access to proprietary algorithm and intellectual property.
- **Multiple Audio Input Sources:** four analog input channels (AI0 to AI3) that can be used simultaneously for omni−directional and directional microphones, telecoils, bone conducting microphones, an input from a remote control interface, or a direct audio input.
- **Signal Detection Mode:** ultra−low−power detection system for signals on any analog inputs.
- **High Throughput Communication Interface:** fast I2C−based and SWJ−DP interfaces for quick download, debugging and general communication.
- **Highly Configurable Interfaces:** two PCM interfaces, three I2C interfaces, two I3C interfaces, two SPI interfaces, a UART interface, an eMMC interface with custom interface buffering, up to 36 GPIOs and 8 LSAD inputs.
- **Asynchronous Sample Rate Converter (ASRC):** provides a mean of synchronizing the audio sample rate between an external radio chip and the Ezairo 8300.
- **Two Audio Sink Clock Counters:** Can be used to measure the timing of the frame periods of an external radio relative to the internal audio sampling rate.
- **Fitting Support:** support for Microcard, HI−PRO 2, HI−PRO USB, QuickCom, and NOAHlink, including NOAHlink's audio streaming feature.
- **Integrated Development Environment (IDE):** a graphical user interface with the capabilities to edit, build and debug applications. It is the main programming interface for the Software Development Kit (SDK).
- **Complete C−development tool chain for the CFX and the LPDSP32.** Includes a C−compiler, an instruction set simulator, an assembler/disassembler, a linker and the IDE debugger integrated in the Ezairo 8300 SDK.
- **Sample Code:** The SDK includes several sample applications and libraries to demonstrate key features of Ezairo 8300. The libraries are typically provided in compiled form with source code also available.
- **Pb−Free**, Halogen Free/BFR Free and are RoHS Compliant.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	–	–	1.98	V	Power supply voltage
VBATOD	–	–	1.98	V	Output driver power supply voltage
VDDO2/3	–	–	1.98	V	I/O supply voltage
VSSA	0	–	–	V	Analog ground
VSSOD	0	–	–	V	Output driver ground
VSSC	0	–	–	V	Digital ground
VSSO	0	–	–	V	I/O ground
Vin	VSSO−0.1	–	VDDO+0.3	V	Digital input pin voltage
	−0.1	–	1.98	V	Digital input pin voltage
Toperation	0	25	50	°C	Operational temperature
Tfunctional	−40	25	85	°C	Extended op. temperature (Note 1)
Tstorage	−40	–	125	°C	Storage temperature
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)					

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The Ezairo 8300 is functional in the extended temperature range, however some parameters may not meet the specifications. E.g. bandgap voltage, oscillator frequency, ADC noise...

Table 2. OVERALL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	0.9	1.25	1.98	V	Supply voltage, measured at the VBAT pin (Note 2)
VBATOD	0.9	1.25	1.98	V	Output driver supply voltage (Note 3)
VDDO2/3	0.9	1.25	1.98	V	I/O voltage (Note 4)
System clock	–	15.36	61.44	MHz	System clock frequency
VDDC retention	0.50	0.53 (Note 5)	–	V	Digital supply voltage, when memories are in retention mode
VDDC limit	0.50	0.51 (Note 5)	–	V	Digital supply voltage limit for adaptive voltage scaling
VDDC active	0.76	0.78 (Note 5)	0.88	V	Digital supply voltage in active mode; used as upper limit for adaptive voltage scaling
VDDM retention	0.50	0.58 (Note 5)	–	V	Memories supply voltage, when memories are in retention mode
VDDM standby	0.76	0.80 (Note 5)	–	V	Memory supply voltage in standby mode
VDDM active	0.76	0.78 (Note 5)	0.88	V	Memory supply voltage in active mode (Note 6)

2. With VBAT below 1.0V, the performance will be degraded. E.g. reduced PSRR, line & load regulations.
3. At system boot, VBATOD is internally connected to VBAT for 5 ms. In case VBATOD is supplied at 1.8 V and VBAT is supplied at 1.25 V, a current of ~130 mA will flow from VBATOD to VBAT. This current does not represent a reliability risk for a typical usage of the chip of 10 boots per day over 10 years.
4. With VDDO below 1.0 V, the performance will be degraded, e.g. the drive strength will be reduced.
5. These values indicate the target trimming values.
6. The VDDM voltage should be higher or equal to the core voltage (VDDC).

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = 1.25 V. The system clock (SYS_CLK) was set to 15.36 MHz. Parameters marked as screened are tested on each chip. Parameters marked as screened with one check are tested on each Ezairo 8300 chip and with two checks are tested on each Ezairo 8310 hybrid module.

CURRENT CONSUMPTION

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Current consumption	I_{VBAT}	CFX load 97%, Arm Cortex−M3 processor load 40%, HEAR load 77%, Filter Engine load 9% 2 ADC @ 20 kHz, 1 OD, 1 LSAD SYS_CLK=15.36 MHz, CCO mult = 2	−	0.7	0.9	mA	✔ ✔ ✔
Standby Current	I_{STDB}	Using **onsemi**'s macro	−	90	120	μA	✔
CFX power consumption	I_{CFX}	Running 31−tap FIR, processing 4 output points in parallel	−	13.7	−	μA/MHz	
Arm Cortex−M3 processor power consumption	I_{CM3}	Running 31−tap FIR, taking advantage of symmetrical coefficients	−	8.3	−	μA/MHz	
HEAR power consumption	I_{HEAR}	Running 31−tap FIR, HEAR FIR_R function	−	18.7	−	μA/MHz	
Filter Engine power consumption	I_{FENG}	Running 31−tap FIR	−	12.0	−	μA/MHz	
LPDSP32 power consumption	$I_{LPDSP32}$	Running G.722 decoding	−	10.0	−	μA/MHz	
NNA power consumption	I_{NNA1}	256−input, 256−output layer, tanh activation function, 8−bit inputs and outputs, 8−bit uncompressed weights	−	17.5	−	μA/MHz	
	I_{NNA2}	256−input, 256−output layer, tanh activation function, 8−bit inputs and outputs, 4−bit logarithmic encoded weights	−	19.7	−	μA/MHz	

NOTE: SYS_CLK = 15.36 MHz using adaptive voltage scaling.

NOTE: Currents are on VBAT at 1.25 V

VREG

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage	VREG	50 μA < I_{LOAD} < 200 μA, trimmed bandgap (Note 7)	0.89	0.9	0.91	V	✔
Load current	I_{LOAD}		−	−	2	mA	
Line regulation	$LINE_{REG}$	I_{LOAD} = 1 mA	−	−	5	mV/V	
Load regulation	$LOAD_{REG}$	5 μA < I_{LOAD} < 2 mA	−	6	10	mV/mA	
PSRR @ 1 kHz	PSRR	I_{LOAD} = 1 mA, VBAT > 1.05 V	80	−	−	dB	

7. VBAT ≥ 1 V is required to have VREG at 0.9 V. Trimming steps: 5 mV. The typical (Typ) value shown for VREG is its target trimming value.

VDDA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage	VDDA	Standby Mode (STBY), I_{LOAD} < 100 μA, VBAT > 0.90 V	1.7	1.8	1.9	V	✔
		Low−Power Mode (LPM), I_{LOAD} = 100 μA, VBAT > 0.92 V	1.7	1.8	1.9	V	
		High-Power Mode (HPM), I_{LOAD} < 4 mA, VBAT > 0.95 V	1.7	1.8	1.9	V	✔
Typical output voltage trimming range	$VDDA_{RANGE}$	LPM, Typical Process, 25°C, VBAT = 1.25 V; I_{LOAD} = 100 μA	1.57	–	1.98	V	
Trimming steps	$VDDA_{STEP}$		–	6.5	–	mV	
Load current	I_{LOAD}	STBY	–	–	100	μA	
		LPM	–	100	500	μA	
		HPM	–	–	4	mA	
Load regulation	$LOAD_{REG}$	LPM, VBAT = 1.20 V; 100 μA < I_{LOAD} < 500 μA	–	4	10	mV/mA	
		HPM, VBAT = 1.20 V; 1 mA < I_{LOAD} < 2 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	SDBY, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 100 μA	–	10	36	mV/V	
		LPM, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 100 μA	–	4	10	mV/V	
		HPM, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 1 mA	–	4	10	mV/V	
PSRR	$VDDA_{PSSR}$	VBAT = 1.2 V; @ 1 kHz	40	–	–	dB	

VDDIF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage (high−power mode)	VDDIF	VBAT > 0.95 V; I_{LOAD} < 5 mA (Note 8)	1.7	1.8	(2xVBAT− 100 mV) (Note 9)	V	✔ ✔
		VBAT > 1.05V; I_{LOAD} < 15 mA	1.7	1.8	(2xVBAT− 200 mV) (Note 9)	V	✔ ✔ ✔
Typical output voltage trimming range	$VDDIF_{RANGE}$		1.57	–	1.98	V	
Trimming steps	$VDDIF_{STEP}$		–	6.5	–	mV	
Load current	I_{LOAD}	Low−power mode	–	–	1	mA	
		High−power mode	–	–	15	mA	✔ ✔
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; HPM, I_{LOAD} = 5 mA	–	5	10	mV/mA	✔ ✔
		VBAT = 1.2 V; LPM; I_{LOAD} = 500 μA	–	17	20	mV/mA	
Line regulation	$LINE_{REG}$	VBAT > 1.2 V; I_{LOAD} = 100 μA	–	4	20	mV/V	
PSRR	$VDDIF_{PSSR}$	VBAT = 1.2 V; @ 1 kHz, I_{LOAD} = 5 mA	30	–	–	dB	

8. VBAT voltage on IC pin
9. VDDIF max can't exceed 1.98 V

NOTE: Low Power Mode (LPM): Switching frequency = 128 kHz / itrim = 0X00
High Power Mode (HPM): Switching frequency = 320 kHz / itrim = 0X10

VMIC

The output voltage on the VMIC pin can be chosen from 5 different sources:

- VMIC regulator powered by VBAT
- VMIC regulator powered by VDDA
- VREG
- VDDA
- VDDIF

VMIC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Switch impedance	$VMIC_{IMP}$	Measured with a 250 μA load current	50	100	250	Ω	
Typical output voltage trimming range	VMIC	Regulator powered by VBAT. Maximum Output: VBAT−0.1 V	0.8	0.95*	1.3	V	✔
		Regulator powered by VDDA	0.8	–	1.3	V	✔
Trimming steps	$VMIC_{STEP}$		–	25	–	mV	
Load current	I_{LOAD}		–	–	500	uA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load regulation	$LOAD_{REG}$		–	5	10	mV/mA	
Regulator VDDA PSRR	$VMIC_{PSSR}$	Regulated from VDDA	60	–	–	dB	
Regulator VBAT PSRR		Regulated from VBAT, VBAT−VMIC > 0.1 V	80	–	–	dB	

NOTE: The resistor between GND_MIC and VSSA is 50 Ohm.
*Typical output voltage trimming.

VDDOD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Typical output voltage trimming range	VDDOD	Maximum Output: VBAT−0.2 V	0.8	1.00*	1.4	V	✔ ✔ ✔
Trimming steps	$VDDOD_{STEP}$		–	25	–	mV	
Load current	I_{LOAD}		–	–	25	mA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load regulation	$LOAD_{REG}$		–	1	10	mV/mA	
PSRR	$VMIC_{PSSR}$		40	–	–	dB	

NOTE: We recommend to always enable the VDDOD regulator. It improves the PSRR when large transient currents are drawn elsewhere in the Ezairo 8300 based system and gives an audio output level that is independent of the battery voltage.
*Typical output voltage trimming.

VDDM/VDDC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Typical output voltage trimming range	$VDDM_{RANGE}$, $VDDC_{RANGE}$	(Note 10)	0.45	–	0.88	V	✔
Trimming steps	$VDDM_{STEP}$, $VDDC_{STEP}$		–	2	–	mV	
Load regulation	$LOAD_{REG}$		–	7	10	mV/mA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load current	I_{LOAD}		–	–	5	mA	
PSRR @ 1 kHz	$VDDM_{PSRR}$, $VDDC_{PSRR}$	VBAT = 1.25 V, VDDC/M = 0.80 V, I_{LOAD} = 500 μA	25	–	–	dB	

10. The voltage of VDDC and VDDM shall not go beyond the values specified in the operating conditions.

BANDGAP REFERENCED REGULATOR TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of −5 to 50°C	−0.5	–	0.5	%	

NOTE: Temperature stability for VREG, VDDA (LPM and HPM), VMIC, VDDOD, VDDC (using the band gap as reference) and VDDM (using the band gap as reference):

PMU REFERENCED REGULATOR TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of −5 to 50°C	−2	–	2	%	

NOTE: Temperature stability for VDDA (STBY), VDDC (using the PMU as reference) and VDDM (using the PMU as reference):

POWER−ON−RESET

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
VBAT startup voltage: High threshold voltage	Vth_{High}		0.68	0.77	0.86	V	✔
VBAT shutdown voltage: Low threshold voltage	Vth_{Low}		0.63	0.72	0.81	V	✔

NOTE: Typical time duration between application of VBAT and first NVM access: 77 ms

INPUT STAGE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Nominal input referred noise 16 kHz SF, RMS	IN_{IRN}	A−weighted 100 Hz−8 kHz, 16 kHz SF, nominal current setting	–	2	4	μVrms	
Nominal input referred noise 32 kHz SF, RMS		A−weighted 100 Hz−16 kHz, 32 kHz SF, maximum current setting	–	3	10 (Note 11)	μVrms	✔
HiQ input referred noise 16 kHz SF, RMS		A−weighted 100 Hz−8 kHz, 16 kHz SF, maximum current setting	–	1.5	3	μVrms	
HiQ input referred noise 48 kHz SF, RMS		A−weighted 20 Hz−20 kHz, 48 kHz SF, maximum current setting	–	3	10 (Note 12)	μVrms	✔
Nominal dynamic range	IN_{DR}	A−weighted 100 Hz−8 kHz, nominal current setting	–	109	–	dB	
HiQ dynamic range		A−weighted 100 Hz−8 kHz, maximum current setting	–	112	–	dB	
Input range	IN_{RANGE}	At VDDA 1.8 V	0	–	1.6	V	
Input impedance	R_{IN}	Nominal and HiQ mode	10	–	–	MΩ	
Peak THDN	IN_{THDN}		–	−85	−70	dB	✔
Channel gain mismatch		Calibrated (using digital gain factor, 1 kHz) or not calibrated	–	–	0.1	dB	
Channel delay mismatch		At 1 kHz (approx. max 0.54 deg)	–	–	1.5	μs	
Ultrasonic immunity, input referred aliased level		A−weighted 100 Hz − 16 kHz aliased level with a −40 dBV input signal swept from 20 kHz to 50 kHz	–	−95	−85	dBV	
Signal detection mode input referred noise		A−weighted 100 Hz−10 kHz, 1 MHz operation, current setting at 0x1 (4 μA)	–	10	20	μVrms	
Microphone bias voltage	MIC_{BIAS}	In order to maximize dynamic range of the input stage, the microphone bias should be set to the typical value	0.2	0.75	1.0	V	

NOTE: Input Stage specifications are A−weighted, bandwidth 100 Hz−fs/2, sampling frequencies 16/32/48 kHz, with ADC_CLK = 3.84 MHz. The CCO multiplier doesn't affect the specifications of the ADC as long as the ADC_CLK is around 4 MHz.

NOTE: The specifications at 20 kHz are between the specifications at 16 and 32 kHz.

11. By characterization, the Max value is 5 μVrms.
12. By characterization, the Max value is 5 μVrms.

OUTPUT STAGE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output resistance	R_{OD}	I_{LOAD} = 1 mA. High and Low side combined.	–	2	5	Ω	✔
Output Dynamic Range	OD_{DR}	High impedance load (>1 kΩ), XSDM0 mode	103	108	–	dB	
		Low impedance speaker mode, 36R load, XSDM0 mode	–	105	–	dB	
		High impedance load (>1 kΩ), OD_DELAY mode	95	100	–	dB	
Peak THD+N	OD_{THDN}	@ 1 kHz, high impedance load (>1 kΩ), XSDM0 mode	–	−72	−61 (Note 13)	dB	✔
		@ 1 kHz, low impedance speaker mode, 36R load, XSDM0 mode	–	−61	–	dB	
		@ 1 kHz, high impedance load (>1 kΩ), OD_DELAY mode	–	−81	−75	dB	
Output noise RMS	OD_{ORN}	At 1.25 V VBATOD; scales linearly with VBATOD	–	–	4.3	μV	
Output Bandwidth	OD_{BW}		–	–	24	kHz	
Maximum output current	I_{OD}	This current can be drawn but with degraded audio quality.	–	–	25	mA	
Power supply rejection ratio (PSRR)	OD_{PSRR}		–	−30	–	dB	
		Using VDDOD regulator	–	−85	−75	dB	

NOTE: Output stage specifications are A−weighted, bandwidth 100 Hz−fs/2, sampling frequencies 16/32/48 kHz, with SDM_CLK = 15.36 MHz, SYS_CLK = 15.36 MHz (CCO multiplier = 1), and with VDDOD = 1.0 V

NOTE: The performances of the OD are optimized when the SDM_CLK operates on the CCO base frequency (the un−multiplied frequency).

13. By characterization, the Max value is −65 dB.

LSAD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
ADC Resolution	$LSAD_{RES}$	Depends on frequency setting	8	12	14	Bits	
Input signal level	$LSAD_{RANGE}$		0	–	1.8	V	✔
Sampling rate	$LSAD_{SF}$	For a sample clock of 128 kHz (20 cycles per measurement)	–	6.4	–	kHz	
lsad_clk frequency	$LSAD_{CLK}$		–	100	128	kHz	
INL	$LSAD_{INL}$		−2	–	+2	mV	
DNL	$LSAD_{DNL}$		−1	–	+1	mV	
Input Impedance	$LSAD_{INI}$		1	–	–	MΩ	

IOs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Voltage level of high input	V_{IH}		–	–	0.7x VDDO	V	✔
Voltage level of low input	V_{IL}		0.3x VDDO	–	–	V	✔
Voltage level of high output	V_{OH}		0.8x VDDO	–	VDDO	V	✔
Voltage level of low output	V_{OL}		VSSO		0.2x VDDO	V	✔
Weak pull−up Impedance	IMP_{WUP}		225	250	275	kΩ	✔
Medium pull−up Impedance	IMP_{MUP}		45	50	60	kΩ	✔
Medium pull−down Impedance	IMP_{MDW}		45	50	60	kΩ	✔

IOs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Strong pull−up Impedance	IMP_{SUP}		0.8	1	1.2	kΩ	✔
Pad Input Delay	IN_{DELAY}	VDDO=1.8V	−	−	0.76	ns	
		VDDO=1.2V	−	−	1.23	ns	
Pad Output Delay	OUT_{DELAY}	VDDO=1.8V 1x drive strength, 1 pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	−	−	1.24	ns	
		VDDO=1.2V 1x drive strength, 1pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	−	−	1.74	ns	
Drive Strength	DRIVE	Configurable with 1x, 2x, 4x, 8x Nominal drive strength: 1 mA	1	−	8	Multiple of the nominal drive strength	
Max Switching Frequency	$IOFR_{Max}$		Maximum SYS_CLK	−	−		
Glitch filter : additional rise delay	$DELAY_{RAISE}$		−	−	169	ns	
Glitch filter : additional fall delay	$DELAY_{FALL}$		−	−	245	ns	

NOTE: DC Characteristics of the digital pad at VDDO 1.08/1.8/1.98V

NOTE: The glitch filter cuts glitches with duration shorter than 50 ns

CURRENT CONTROLLED OSCILLATOR (CCO)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Recommended Working Frequency	SYS_CLK	For recommended VDDC and VDDM	2.56	−	61.44	MHz	
Boot frequency	SYS_CLK		5	7.68	10	MHz	✔ ✔ ✔
Oscillator frequency trimming precision			−	0.10	0.20	%	
Frequency stability in temperature		Temp: 0°C and 50°C. After calibration at room temperature (25°C)	−1.5	−	1.5	%	
		Temp: −40°C and 85°C. After calibration at room temperature (25°C)	−4	−	4	%	
Period jitter (rms)		RMS, at 5.12 MHz, before multiplication	−	−	200	ps	
		RMS, at 5.12 MHz, after multiplied by 2 and divided by a multiple of 2	−	−	200	ps	
		RMS, at 5.12 MHz, after multiplied by 4 and divided by a multiple of 4	−	−	200	ps	
Output duty cycle		With multiplier setting 1x or 2x	45	−	55	%	
		With multiplier setting 4x	40	−	60	%	
Max frequency		Un−multiplied	−	30	−	MHz	

LOW DELAY PATH (using the low delay path of the Filter Engine)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Analog to analog delay		Fs = 48 kHz FENG delay: one sample	–	10.4	–	μs	

NVM (LE25S161)

Description	Symbol	Conditions	Min	Typ	Max	Unit	Sceened
Rewrite cylces, per Sector	cyc_{RW}	Per LE25161 datasheet	100'000			Cycles/ Sector	
Data Retention	t_{DRET}	Per LE25161 datasheet	20			year	
Program Mode Operating Current	I_{CCPPL}	Per LE25161 datasheet		5		mA	
Read Mode Operating Current	I_{CCR}	Per LE25161 datasheet		3.5		mA	

Ezairo 8310 System Diagram

Figure 1 is a simplified diagram of the hybrid system that shows the major internal functional blocks and possible external

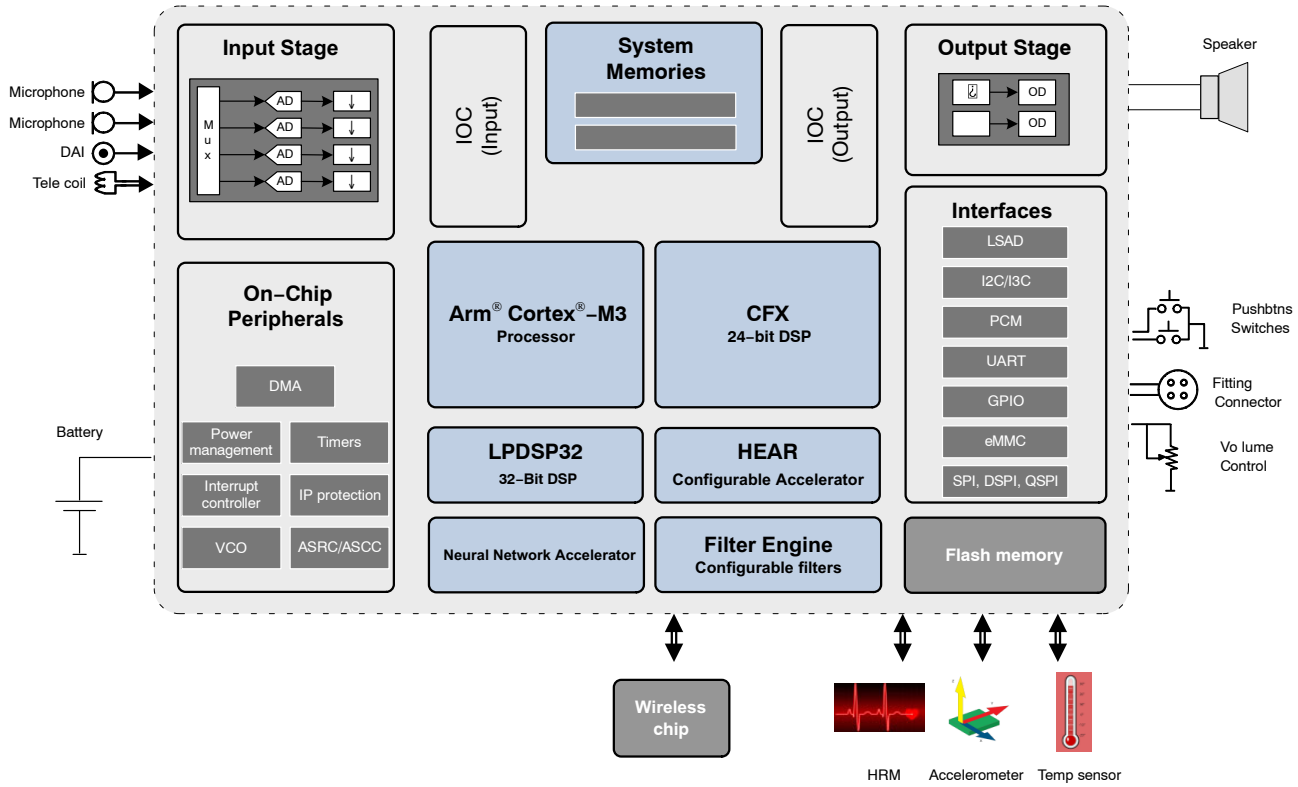


Figure 1. Ezairo 8310 Hybrid System Diagram

ARCHITECTURE OVERVIEW

The Ezairo 8300 system is an asymmetric 6−core architecture, mixed−signal system−on−chip designed specifically for the audio processing needs ultra−lower power portable devices. It centers around 6 processing cores: the CFX Digital Signal Processor (DSP), the Arm Cortex−M3 Processor, the LPDSP32 Digital Signal Processor (DSP), the HEAR Configurable Accelerator, the Filter Engine and the Neural Network Accelerator.

CFX DSP Core

The CFX DSP is a user−programmable general−purpose DSP core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. It is able to perform two MACs, two memory operations and two pointer updates per cycle, making it well−suited to computationally intensive algorithms.

The CFX DSP is used for custom signal processing applications. The CFX DSP core can also be used as the master of the Ezairo 8300 SoC, by configuring the system and the other cores, by managing the Interrupts and by coordinating the flow of signal data progressing through the system.

The CFX features:

- Dual−MAC 24−bit load−store DSP core
- Four 56−bit accumulators
- Four 24−bit input registers
- Support for hardware loops nested up to four deep
- Combined XY memory space (48 bits wide)
- Dual address generator units
- A wide range of addressing modes:
  - Direct
  - Indirect with post−modification
  - Modulo addressing
  - Bit reverse

Software development on the CFX is done in C or assembly, and the development tools are available in the Ezairo 8300 SDK.

In cases where the Arm Cortex−M3 processor is used as the master of the system, the CFX is slave to the Arm Cortex−M3 processor. The inter−processor communication methods between the CFX processor and the rest of Ezairo 8300 are based on shared memories and interrupts.

CFX DSP Architecture

The CFX employs a parallel instruction set for simultaneous control of multiple computation units. The DSP can execute up to four computation operations in parallel with two data transfers (including rounding and/or saturation as well as complex address updates), while simultaneously changing control flow.

The CFX architecture encompasses various memory types and sizes, peripherals, interrupt controllers, and interfaces.

Arm Cortex−M3 Processor

The Arm Cortex−M3 processor is a low−power processor that features low gate count, low interrupt latency, and low−cost debugging. It is intended for deeply embedded applications that require fast interrupt response features.

GNU tools provide build and link support for C programs that run on the Arm Cortex−M3 processor.

The Arm Cortex−M3 processor implements the ARMv7−M architecture. For power management, the processor can be placed into a sleep mode under firmware control in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) continues to run to enable exiting sleep on an interrupt.

The Arm Cortex−M3 processor typically performs one or more of the following roles:

- The system master, configuring the system and the other cores, by managing the interrupts, and by coordinating the flow of signal data progressing through the system
- A coprocessor to the CFX DSP that provides additional microcontroller computation for interface drivers and protocols executing on those interfaces
- A controller for managing hardware acceleration peripherals such as the Reed−Solomon, G.722 blocks, the asynchronous sample rate converter (ASRC), the audio sink clock counters (ASCC), the neural network accelerator (NNA), or the LPDSP32 DSP (which is expected to be used for codecs, a neural network, and similar use cases)

In cases where the CFX is used as the master of the system, the Arm Cortex−M3 processor is slave to the CFX. The inter−processor communication methods between the Arm Cortex−M3 processor and the rest of Ezairo 8300 are based on shared memories and interrupts.

HEAR Configurable Accelerator

The HEAR coprocessor is designed to perform both common signal processing operations and complex standard filterbanks such as the WOLA filterbank, reducing the load on the system programmable DSP cores.

The HEAR Configurable Accelerator is a highly optimized signal processing engine that is configured through the CFX or Arm Cortex−M3 processor. It offers high speed, high flexibility and high performance, while maintaining low power consumption. For added computing precision, the HEAR supports block floating point processing. Configuration of the HEAR is performed using the HEAR Configuration Tool (HCT). For further information on the usage of the HEAR, refer to the *HEAR Configurable Accelerator Reference Manual*.

The HEAR is optimized for advanced algorithms including but not limited to the following:

- Dynamic range compression
- Directional processing

- Feedback cancellation
- Noise reduction

To execute these and other algorithms efficiently, the HEAR excels at the following:

- Processing using a weighted overlap add (WOLA) filterbank
- Time domain filtering
- Subband filtering
- Attack/release filtering
- Vector addition/subtraction/multiplication
- Signal statistics (such as average, variance and correlation)

Filter Engine

The Filter Engine is a core that provides low−delay path and basic filtering capabilities for the Ezairo 8300 system.

The Filter Engine can implement filters (either FIR or IIR) with a total of up to 320 coefficients. FIR filters are implemented using a direct−form structure. IIR filters are implemented with a cascade of second−order sections (biquads), each implemented as a direct−form I filter.

The Filter Engine is programmable, but does not include direct debugging access. The CFX and the Arm Cortex−M3 Processor can monitor the Filter Engine state through control and configuration registers on the program memory bus.

LPDSP32 DSP

LPDSP32 is a C−programmable, 32−bit DSP developed by **onsemi**. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32−bit) and double precision (64−bit) arithmetic.

LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks such as audio codecs that might be required for wireless audio communication tasks, Artificial Intelligence (AI) functions, and other advanced developments requiring the additional processing power that this core provides. The advanced architecture also provides:

- Two 72−bit ALUs capable of doing single and double precision arithmetic and logical operations
- Two 32−bit integer/fractional multipliers
- Four 64−bit accumulators with 8−bit overflow (extension bits)

The LPDSP32 relies on the CFX DSP or the Arm Cortex−M3 processor to initialize its memories and peripherals. Once initialized, the CFX DSP and/or the Arm Cortex−M3 processor control the LPDSP32 DSP's execution state.

Software development on the LPDSP32 is done in C.

Neural Network Accelerator (NNA)

The Neural Network Accelerator (NNA) is a hardware accelerator block that allows complex neural networks to run in an energy efficient manner. The accelerator can execute a single layer of a fully populated or sparsely populated neural network in a single task without any processor intervention. Layers with up to 1023 inputs and 1023 outputs are supported.

The NNA contains 16 multipliers, 16 accumulators, 16 input registers and 16 coefficient registers. It includes input and coefficient "fetchers" that, once configured, manage the data and coefficients memory access automatically. Support for coefficient compression/decompression and pruning is included and help minimize the amount of coefficient needed.

Other key components of the Ezairo 8300 are:

Memory systems: The memory systems provided by the Ezairo 8300 system are constructed using a number of memories (memory instances), memory buses, memory controllers and memory arbiters. These memories and other memory−mapped elements are addressable from the CFX DSP and the Arm Cortex−M3 processor through a set of memory spaces (also known as address spaces).

FIFO Controller: The Ezairo 8300 system's FIFO controller provides the ability to define up to 32 FIFO buffers.

Input/Output Controllers (IOC): The IOCs are responsible for handling input/output audio data. Samples can be routed along a number of different paths using the multiplexing options available in the Ezairo 8300 system.

Direct Memory Access (DMA) Controller: The direct memory access controller (DMA) module allows background transfers between components on the peripheral bus (referred to in this section as peripherals) and memories without any processor intervention. This allows the processors to be used for other computational needs while enabling high speed sustained transfers to and from the peripherals/memories. The DMA has 8 independent configurable channels.

Input Stage: The input stage of an Ezairo 8300 provides four audio input channels that supply signal data to the rest of the Ezairo 8300 system.

Output Stage: The output stage of Ezairo 8300 provides two audio output channels that post−process signal data from the rest of the Ezairo 8300 system, and provide it to external receivers or speakers.

General Purpose Input/Output (GPIO) Pads: The Ezairo 8310 system offers 20 general purpose input/output (GPIO) pads that can be configured:

- To support the external interfaces, output clocks, and other I/Os
- As general−purpose I/Os (GPIO)
- Analog input/output function

The 20 GPIOs are split into four power domains. The voltages for these 4 power domains are given by:

- VDDO1 (GPIO5, GPIO7 to GPIO11) is supplied by VDDIF

- VDDO2 (GPIO 18 to GPIO 23) is connected externally to the Ezairo 8310 hybrid
- VDDO3 (GPIO 24 to GPIO 26, GPIO 28) is connected externally to the Ezairo 8310 hybrid
- VDDO4 (GPIO 30 to GPIO 33, GPIO 35) is supplied by VBAT

The SCL and SDA pads are connected to the VDDO4 power domain.

It is possible to connect the Ezairo 8310 to an additional SPI based NVM. The following GPIOs can be used:

- GPIO 0 is connected to the SCK signal of the LE25S161 flash internally and connected externally to the Ezairo 8310 hybrid
- GPIO 2 is connected to the SI signal of the LE25S161 flash internally and connected externally to the Ezairo 8310 hybrid
- GPIO 3 is connected to the SO signal of the LE25S161 flash internally and connected externally to the Ezairo 8310 hybrid

The Chip Select signal of an additional SPI based NVM will be controlled with any other available GPIOs.

External Interfaces:

- **General−Purpose Input/Output (GPIO):** Ezairo 8310 can configure any, or all, of the 20 GPIO pads as software−controlled general−purpose GPIO pads.
- **PCM Interface:** The Ezairo 8300 system includes two highly−configurable pulse code modulation (PCM) interfaces that can be used to stream signal, control and configuration data in and out of the device. The PCM interface can be configured in I2S mode.
- **SPI Interface:** The Ezairo 8300 system includes two Serial Peripheral Interfaces (SPIs). Each SPI interface supports single and dual I/O modes, as well as the ability to add two additional I/O pins in a quad I/O mode.
- **UART Interface:** The general−purpose UART interface provides support for communicating with devices that use standard UART and RS−232 transmission protocols.
- **Low−Speed A/D Converters (LSAD):** The purpose of the LSAD converters is to sample voltages that typically change slowly, such as the voltage associated with a potentiometer−based volume control.
- **I2C Interface:** The Ezairo 8300 includes 3 instances of I2C interface, which are compatible with the Inter−IC Bus Specification from NXP Semiconductors.
- **I3C Interface:** The Ezairo 8300 includes 2 instances of I3C interface, which are compatible with the Improved Inter−IC Bus Specification from the MIPI Alliance.
- **eMMC Interface:** eMMC memory (Embedded MultiMedia Card memory) is a low−cost, high performance Flash memory that is designed for a wide range of applications in consumer electronics such as mobile phones, handheld computers, navigational systems, portable gaming and even industrial uses.

Debug Ports:

- **I2C Debug Ports for the CFX and the Arm Cortex−M3:** The I2C debug ports for the Ezairo 8300 system provide both the CFX DSP and Arm Cortex−M3 processor with a full debugging capacity. The CFX DSP debug port coexists with the Arm Cortex−M3 processor debug port on the same I2C bus. One of the three general purpose I2C interface can be used on the same bus. Each debug port will respond to debug commands on its I2C address.
- **SWJ−DP Debug Port for the Arm Cortex−M3:** The Ezairo 8300 system contains a standard Core Sight SWJ−DP debug port for the Arm Cortex−M3 processor. This debug controller is used to provide access to all of the Arm Cortex−M3 processor registers, and to all of the Ezairo 8300 memories through the memory buses attached to the Arm Cortex−M3 processor. By default, the SWJ−DP is accessed using the JTAG connection that uses GPIOs 30 to 33 to form a 4−wire JTAG interface. This debug port can be reconfigured for serial−wire mode using only GPIOs 30 and 31. The Arm Cortex−M3 processor's SWJ−DP debug port can be used as a bridge to the CFX I2C debug port through a memory−mapped register.
- **Standard JTAG debug port for the LPDSP32:** The LPDSP32 is supported by a JTAG debug interface that can be assigned to a set of GPIO pads.

Other Peripherals:

- **Clock−Generation Circuitry and Synchronization:** The main system clock is typically generated by a current−controlled oscillator (CCO) that can be configured for frequencies from 1.28 MHz to 61.44 MHz. Other needed clocks are derived from the main system clock. An Asynchronous Sample Rate Converter (ASRC) and Audio Sink Clock Counters blocks to provide a means of synchronizing the audio sample rate between the radio link and the host device.
- **Power Supervisory Unit:** The power supervisory unit monitors the battery supply voltage (VBAT) and the internal analog and digital supply voltages (VDDA, VDDC, VDDM), safely shutting down the system without user intervention when the supply voltages are below the thresholds required for valid system operation.
- **Power−on−Reset (POR):** The Ezairo 8300 device uses a power−on−reset (POR) sequence to ensure proper system behavior during startup, and to ensure proper system configuration after startup.

Ezairo 8310 HYBRID INTERFACE SPECIFICATIONS

A total of 49 pads are present on the Ezairo 8310 hybrid. These pads are the interfaces between the hybrid and the other components in the hearing aid. They are listed in the table below.

Ball Number	Hybrid Pad Name	Hybrid Pad Description
A1	DGND	Digital Core Ground
A2	SPI_SO	SPI Serial Out
A3	SPI_SI	SPI Serial In
A4	GPIO9	Digital input / output 9
A5	GPIO10	Digital input / output 10
A6	GPIO20	Digital input / output 20
A7	GPIO19	Digital input / output 19
A8	GPIO21	Digital input / output 21
A9	GPIO23	Digital input / output 23
A10	GPIO22	Digital input / output 22
B1	VDDIF	Interface power supply
B2	GPIO5	Digital input / output 5
B3	SPI_SCK	SPI Clock
B4	GPIO8	Digital input / output 8
B5	GPIO11	Digital input / output 11
B6	GPIO26	Digital input / output 26
B7	GPIO18	Digital input / output 18
B8	GPIO24	Digital input / output 24
B9	GPIO25	Digital input / output 25
B10	VDDO2	I/O domain 2 power supply
C1	DGND	Digital Core Ground
C2	AGND	Analog ground
C3	GNDMIC	Input Transducer ground
C4	DGND	Digital Core Ground
C5	GPIO31	Digital input / output 31
C6	GPIO30	Digital input / output 30
C7	GPIO28	Digital input / output 28
C8	GPIO32	Digital input / output 32
C9	VDDO3	I/O domain 3 power supply
C10	VBAT	Battery input voltage
D1	AI3	ADC analog input 3
D2	VREG	Regulated voltage output
D3	VMIC	Microphone power supply
D4	DGND	Digital Core Ground
D5	GPIO35	Digital input / output 35
D6	GPIO33	Digital input / output 33
D7	DGND	Digital Core Ground
D8	NRESET	Reset Pin
D9	SDA	Debug port data

Ball Number	Hybrid Pad Name	Hybrid Pad Description
D10	VBATOD	Output driver power supply
E1	AI2	ADC analog input 2
E2	AI1	ADC analog input 1
E3	AI0	ADC analog input 0
E5	RCVR0P	Output Driver: Receiver Output 0 Positive
E6	RCVR0N	Output Driver: Receiver Output 0 Negative
E7	RCVR1P	Output Driver: Receiver Output 1 Positive
E8	RCVR1N	Output Driver: Receiver Output 1 Negative
E9	SCL	Debug port clock
E10	VSSOD	Output driver ground

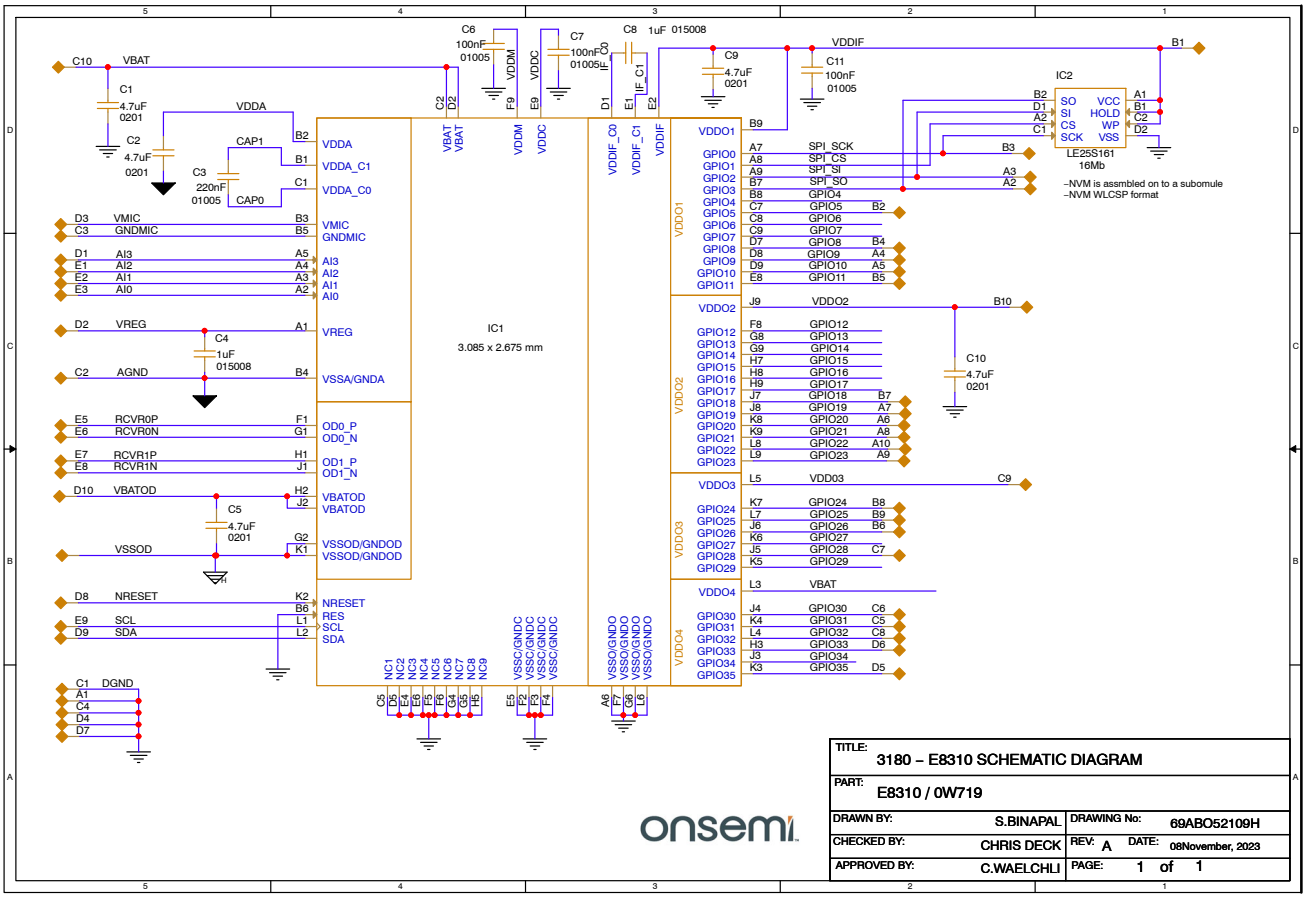


Figure 2. Ezairo 8310 Hybrid Schematics

Packaging and Manufacturing

- Ultra−miniature form factor: suitable for all hearing aid styles including CIC, ITE, RITE, BTE, and mini−BTE.
- Re−flowable: the Ezairo 8310 hybrid is re−flowable onto FR4 and other substrates.
- RoHS compliant: the Ezairo 8310 hybrid complies with the RoHS directive.

System Identification

System identification is used to identify different system components. This information can be retrieved using any of the supported communication box and protocol software provided by **onsemi**.

For the Ezairo 8300 chip, the key identifier components and values are as follows:

- Chip Family: 0x0A
- Chip Version: 0x01
- Chip Revision: 0x0101

The hybrid ID can be found in the manufacturing area of the NVM at address **0x00F1** to **0x00F2** (2 bytes => 16 bits).

- Hybrid ID: 0x00A0

Solder Information

The Ezairo 8310 hybrid is constructed with all RoHS compliant material with bump metallization of SAC305 (Sn96.5/Ag3.0/Cu0.5) solder and should therefore be reflowed accordingly. This hybrid device is Moisture Sensitive Class MSL3, 260°C and must be stored and handled accordingly. For soldering guidelines, please refer to the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D). Hand soldering is not recommended for this part.

Electrostatic Discharge (ESD) Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Development Tools

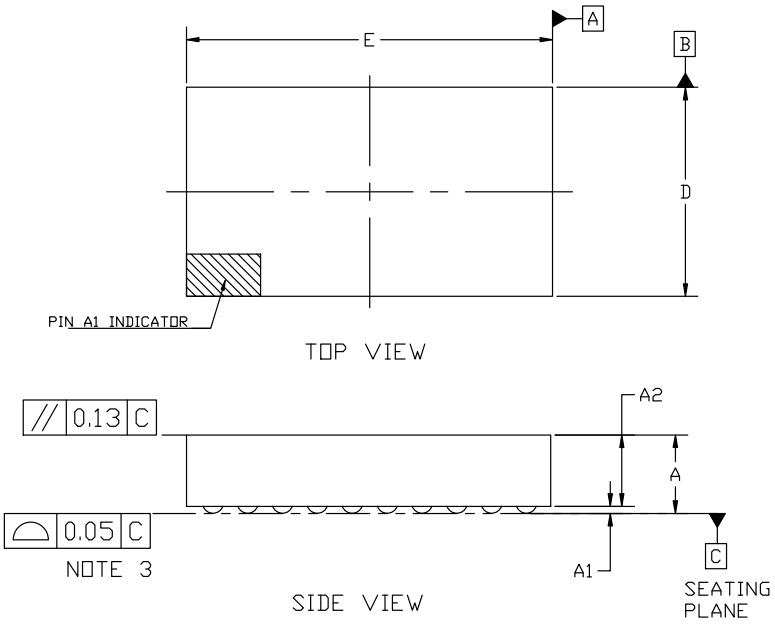
A full suite of comprehensive tools is available to assist software developers from the initial concept and technology assessment through to prototyping and product launch.

Application development and communication tools, as well as an Evaluation and Development Kit (EDK) facilitate the development of advanced algorithms on the Ezairo 8310 hybrid.

EZAIRO 8310 Hybrid

PACKAGE DIMENSIONS

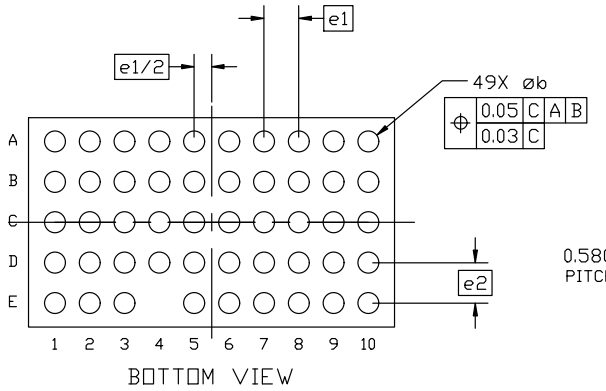
SIP49 3.00x5.25
CASE 127FH
ISSUE A

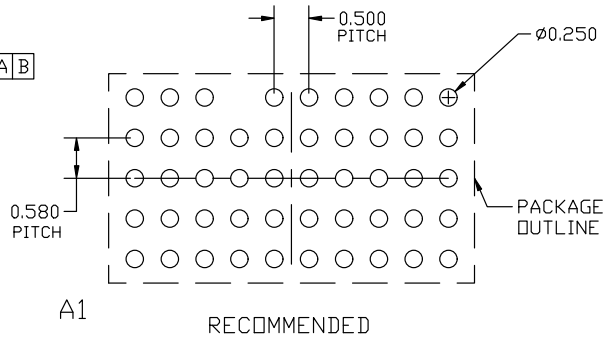


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE PADS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.275
A1	0.050	0.100	0.150
A2	0.925	1.025	1.125
b	0.250	0.300	0.350
D	2.875	3.000	3.125
E	5.125	5.250	5.375
e1	0.500 BSC		
e2	0.580 BSC		





* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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