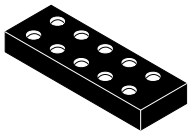
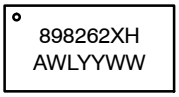
New Closed Loop Auto Focus (AF) Driver

LC898262XHTBG



WLCSP10 0.77x2.27x0.33
CASE 567YK

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

Overview

This LSI is New Closed Loop Auto Focus control LSI. It consists of sensorless damping control function, temperature compensation function, and bi−direction constant current driver.

Features

- Built−in Equalizer Circuit Using Digital Operation
  - Sensorless Damping Control Function
  - Any Coefficient can be Specified by 2−wire Serial I/F (TWIF)
- Temperature Compensation Function
- 2−wire Serial Interface (The Communication Protocol is Compatible with I^2C.)
  - 8 Selectable Slave Addresses
    - 50h (W) / 51h (R)
    - 74h (W) / 75h (R)
    - E8h (W) / E9h (R)
    - E4h (W) / E5h (R) [Factory−configured]
    - Other 4 Addresses can be Selected
- Digital Gyro I/F (SPI Master / Slave)
- Built−in A/D Converter
- Built−in D/A Converter
- Built−in Amplifier
- Built−in EEPROM
  - 64 byte (16 byte/Page)
- Built−in OSC
- Built−in Bi−Direction Constant Current Driver
  - 130 mA
  - 150 mA (High Current Mode)
- Package
  - WL−CSP 10−pin (2 x 5 Pin), Thickness Max 0.35 mm, with Backside Coat
  - Pb−Free, Halogen Free/BFR Free and RoHS Compliant
- Supply Voltage
  - VDD (2.6 V to 3.3 V)
  - IOVDD (1.7 V to 3.3 V)

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

Symbol	Description
I	Input
O	Output
P	Power supply, GND
NC	Not connect
B	Bidirection

- 2−wire serial interface
  SCL I 2−wire serial interface clock pin
  SDA B 2−wire serial interface data pin
- Digital gyro interface
  SSB B Digital Gyro Data I/F Chip Select
  SCLK B Digital Gyro Data I/F Clock
  SDIO B Digital Gyro Data I/F Data InOut
- Driver interface
  OUT1 O Driver output (to Actuator)
  OUT2 O Driver output (to Actuator)
- Power supply pin
  VDD P Power Supply
  VSS P GND
  IOVDD P I/O Power of Digital Gyro Data I/F (1.7 V to 3.3 V)

**Process When Pins Are Not Used*

PIN TYPE “O” – Ensure that it is set to OPEN.
PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.
(Please contact **onsemi** for more information about selection of VDD or VSS)
PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us
Note that incorrect processing of unused pins may result in defects.

PIN LAYOUT

Circuit Name	Number of PINs
Driver	2
Power	3
I/O (VDD)	2
I/O (IOVDD)	3

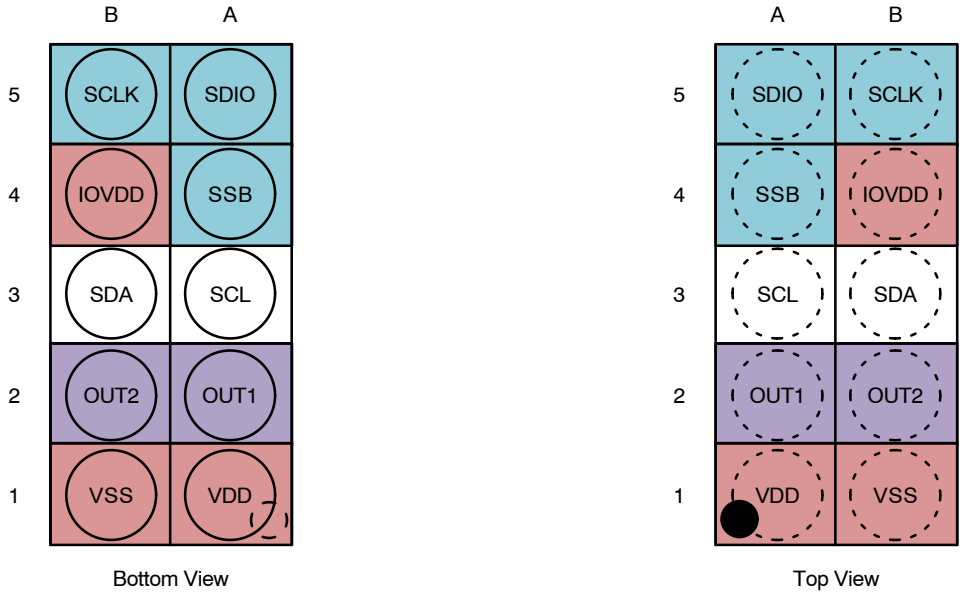
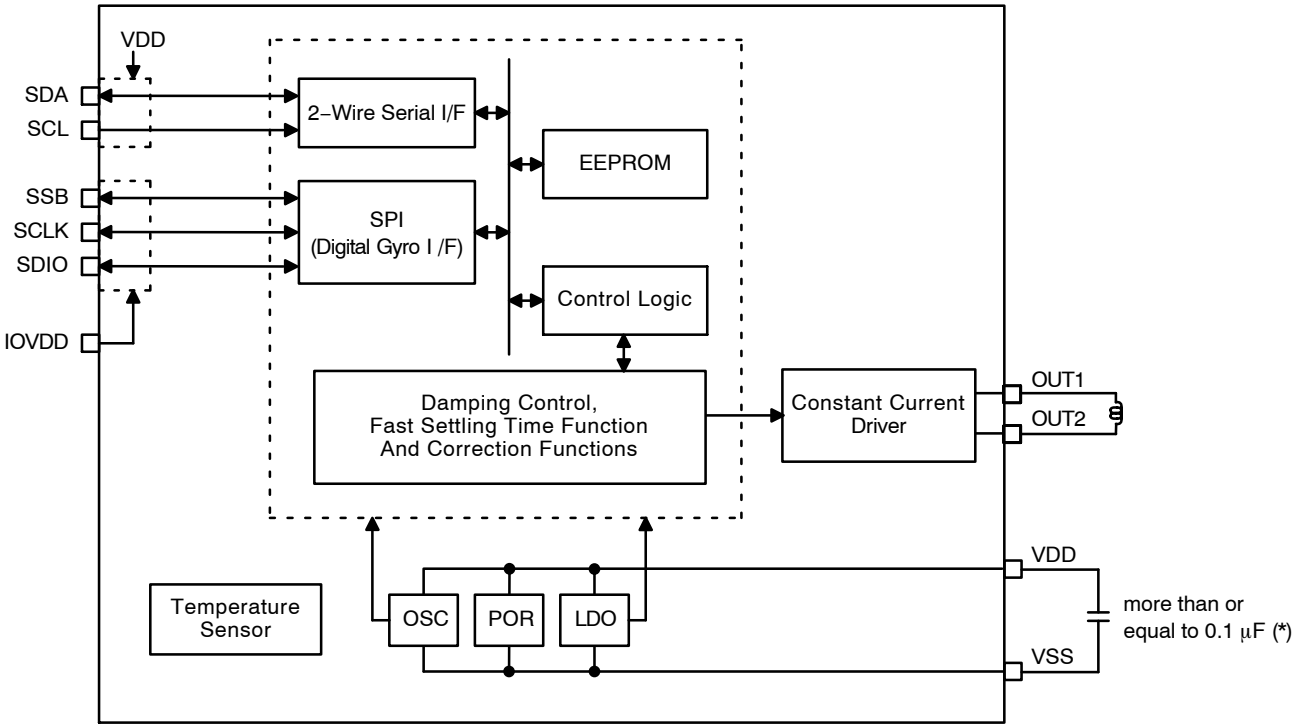


Figure 1. Pin Layout

BLOCK DIAGRAM



*Consider capacitance of capacitor between VDD and VSS. According to power source environment, attach an additional capacitor in camera module.

Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

Table 2. ABSOLUTE MAXIMUM RATINGS (VSS = 0 V)

Symbol	Parameter	Condition	Rating	Unit
V_{DD} max	Supply Voltage (VDD)	Ta ≤ 25°C	−0.3 to 4.6	V
V_I1 max, V_O1 max	Input/Output Voltage (SCL,SDA)	Ta ≤ 25°C	−0.3 to V_{DD} + 0.3	V
V_{IO} max	Supply Voltage (IOVDD)	Ta ≤ 25°C	−0.3 to 4.6	V
V_I2 max, V_O2 max	Input/Output Voltage (SSB,SCLK,SDIO)	Ta ≤ 25°C	−0.3 to V_{IO} + 0.3	V
Tstg	Storage Ambient Temperature		−55 to +125	°C
Topr	Operating Ambient Temperature		−30 to +70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS (TA = −30 to +70°C, VSS = 0 V)

Symbol	Parameter	Min	Max	Max	Unit
V_{DD}	Supply Voltage (VDD)	2.6	2.8	3.3	V
V_I1	Input Voltage Range (SCL,SDA)	0	−	V_{DD}	V
V_{IO}	Supply Voltage (IOVDD)	1.7	1.8	3.3	V
V_I2	Input Voltage Range (SSB,SCLK,SDIO)	0	−	V_{IO}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC CHARACTERISTICS (VSS = 0 V, VDD = 2.6 V to 3.3 V, TA = −30 to +70°C)

Symbol	Parameter	Condition	Min	Max	Max	Unit	Applicable Pins
$V_{IH}1$	High−level Input Voltage	CMOS schmitt	1.4	−	−	V	SCL, SDA
$V_{IL}1$	Low−level Input Voltage		−	−	0.4	V	
$V_{OL}1$	Low−level Output Voltage	IOL= 3 mA	−	−	0.2	V	SDA
$V_{IH}2$	High−level Input Voltage	CMOS schmitt	0.7 x V_{IO}	−	−	V	SSB, SCLK, SDIO
$V_{IL}2$	Low−level Input Voltage		−	−	0.3 x V_{IO}	V	
$V_{OH}2$	High−level Output Voltage	IOH= −3 mA	V_{IO} − 0.2	−	−	V	
$V_{OL}2$	Low−level Output Voltage	IOL= 3 mA	−	−	0.2	V	
R_{UP}	Pull Up Resistor	V_{IO} = 1.8 V	50	−	250	kΩ	
R_{DN}	Pull Down Resistor	V_{IO} = 1.8 V	50	−	250	kΩ	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. DRIVER OUTPUT (OUT1, OUT2) (VSS = 0 V, VDD = 2.8 V, TA = 25°C)

Symbol	Parameter	Condition	Min	Max	Max	Unit	Applicable Pins
Ifull	Maximum Current		123.5	130	136.5	mA	OUT1, OUT2
IfullHC	Maximum Current (High Current Mode)		138	150	162	mA	OUT1, OUT2

Table 6. NON−VOLATILE MEMORY CHARACTERISICS

Symbol	Parameter	Condition	Min	Max	Max	Unit	Applicable Circuits
EN	Endurance	(Note 1)	−	−	1000	Cycles	EEPROM
RT	Data Retention		10	−	−	Years	
tWT	Write Time		−	−	20	ms	

1. The number of write access executable times per page

AC CHARACTERISTICS

VDD Supply Timing

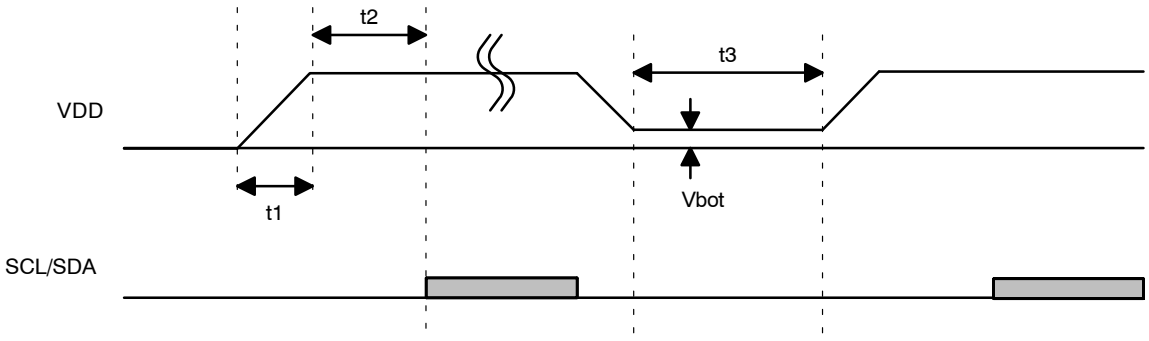


Figure 3. VDD Supply Timing

It is available to use 2−wire serial interface 5ms later for Power On Reset of VDD.

Table 7. VDD SUPPLY TIMING

Symbol	Item	Min	Typ	Max	Unit
t1	VDD Turn On Time	−	−	3	ms
t2	2−wire Serial Interface Start Time from VDD On	5	−	−	ms
t3	VDD Off Time	100	−	−	ms
Vbot	Bottom Voltage	−	−	0.1	V

Injection order between IOVDD and VDD is below.

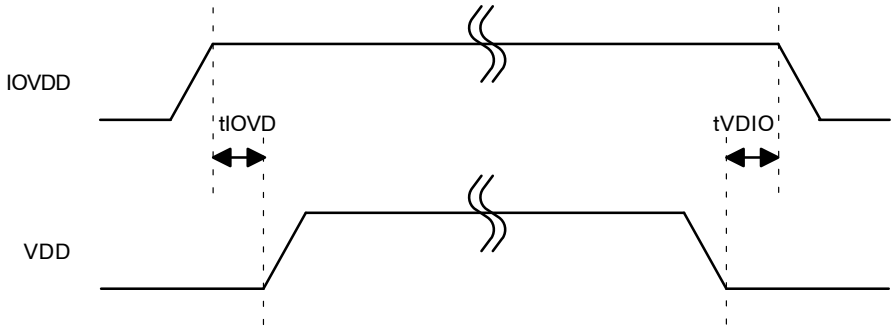


Figure 4. IOVDD Supply Timing

Table 8. IOVDD SUPPLY TIMING

Symbol	Item	Min	Typ	Max	Unit
tIOVD	IOVDD ON to VDD ON	0	−	−	ms
tVDIO	VDD OFF to IOVDD OFF	0	−	−	ms

At the time of power off, SCL, SDA, SCLK and SDIO tolerate 3.3 V input, and SSB pin needs to be low level.

AC Specification of TWIF

Figure 5 shows interface timing definition and Table 9 shows electric characteristics

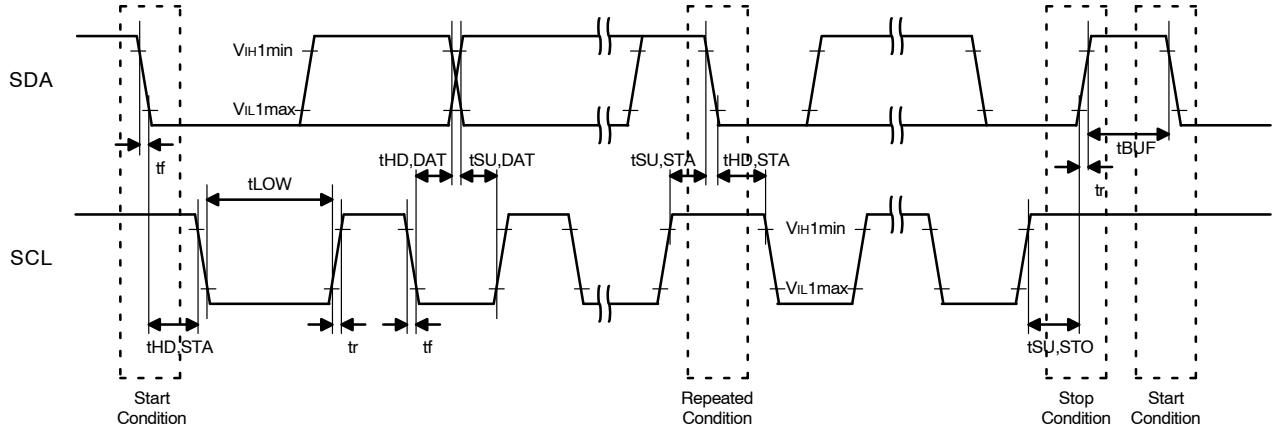


Figure 5. 2−wire Serial Interface Timing Definition

Table 9. 2−WIRE SERIAL INTERFACE AC CHARACTERISTICS

Symbol	Item	Pin Name	Fast−mode			Fast−mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
FSCL	SCL Clock Frequency	SCL	−	−	400	−	−	1000	kHz
tHD,STA	START Condition Hold Time	SCL SDA	0.6	−	−	0.26	−	−	μs
tLOW	SCL Clock Low Period	SCL	1.3	−	−	0.5	−	−	μs
tHIGH	SCL Clock High Period	SCL	0.6	−	−	0.26	−	−	μs
tSU,STA	Setup Time for Repetition START Condition	SCL SDA	0.6	−	−	0.26	−	−	μs
tHD,DAT	Data Hold Time	SCL SDA	0 (Note 2)	−	0.9	0 (Note 2)	−	−	μs
tSU,DAT	Data Setup Time	SCL SDA	100	−	−	50	−	−	ns
tr	SDA, SCL Rising Time	SCL SDA	−	−	300	−	−	120	ns
tf	SDA, SCL Falling Time	SCL SDA	−	−	300	−	−	120	ns
tSU,STO	STOP Condition Setup Time	SCL SDA	0.6	−	−	0.26	−	−	μs
tBUF	Bus Free Time between STOP and START	SCL SDA	1.3	−	−	0.5	−	−	μs

2. This LSI is designed for a condition with typ. 20ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

AC Specification of Digital Gyro I/F (Master)

Figure 6 shows interface timing definition and Table 10 shows electric characteristics.

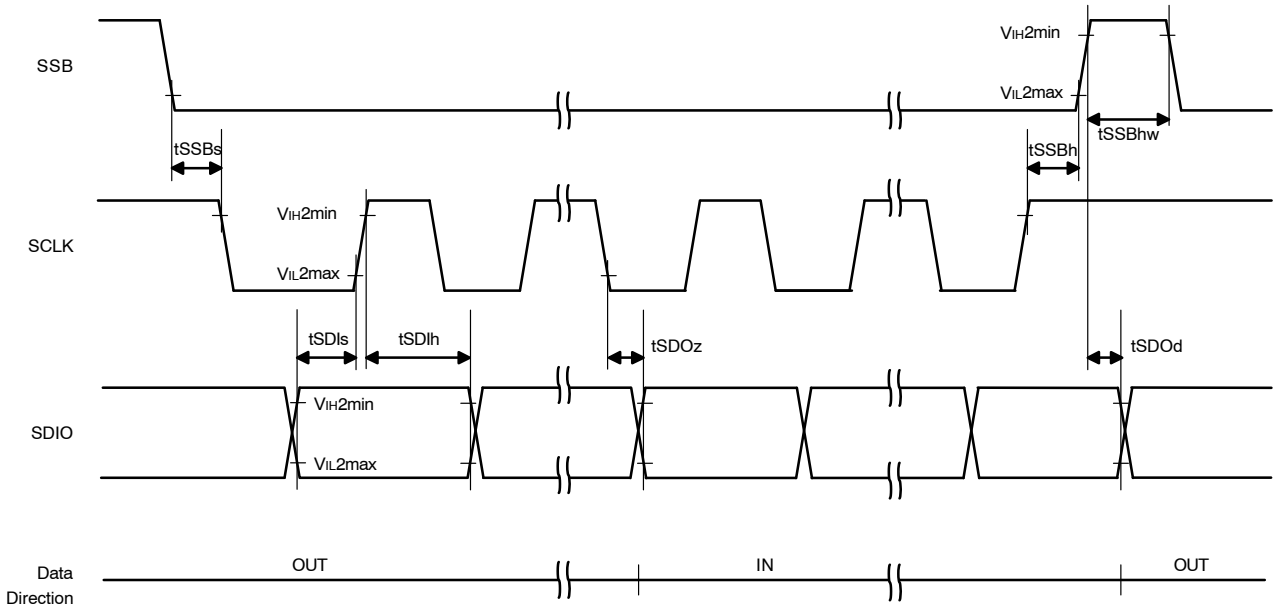


Figure 6. Digital Gyro interface (Master) Timing Definition

Table 10. DIGITAL GYRO INTERFACE(MASTER) AC CHARACTERISTICS

Symbol	Item	Pin Name	Min	Typ	Max	Unit
FSCLK	SCLK Clock Frequency	SCLK	3.8	4	4.2	MHz
fSCLKdu	SCLK Duty	SCLK	40	–	60	%
tSSBhw	SSB High Period	SSB	1.35	–	–	μs
tSSBs	Setup Time for SCLK (F) of SSB	SSB SCLK	50	–	–	ns
tSSBh	Hold Time for SCLK (R) of SSB	SCLK SSB	160	–	–	ns
tSDIs	Setup Time for SCLK (R) of SDIO	SCLK SDIO	50	–	–	ns
tSDIh	Hold Time for SCLK (R) of SDIO	SCLK SDIO	50	–	–	ns
tSDOz	Delay Time from SCLK (F) to SDIO Invalid	SCLK SDIO	–	–	20	ns
tSDOd	Delay Time from SSB (R) to SDIO Update	SSB SDIO	–	–	20	ns
Cld	Load Capacitance	all	–	–	10	pF

AC Specification of Digital Gyro I/F (Slave)

Figure 7 shows interface timing definition and Table 11 shows electric characteristics.

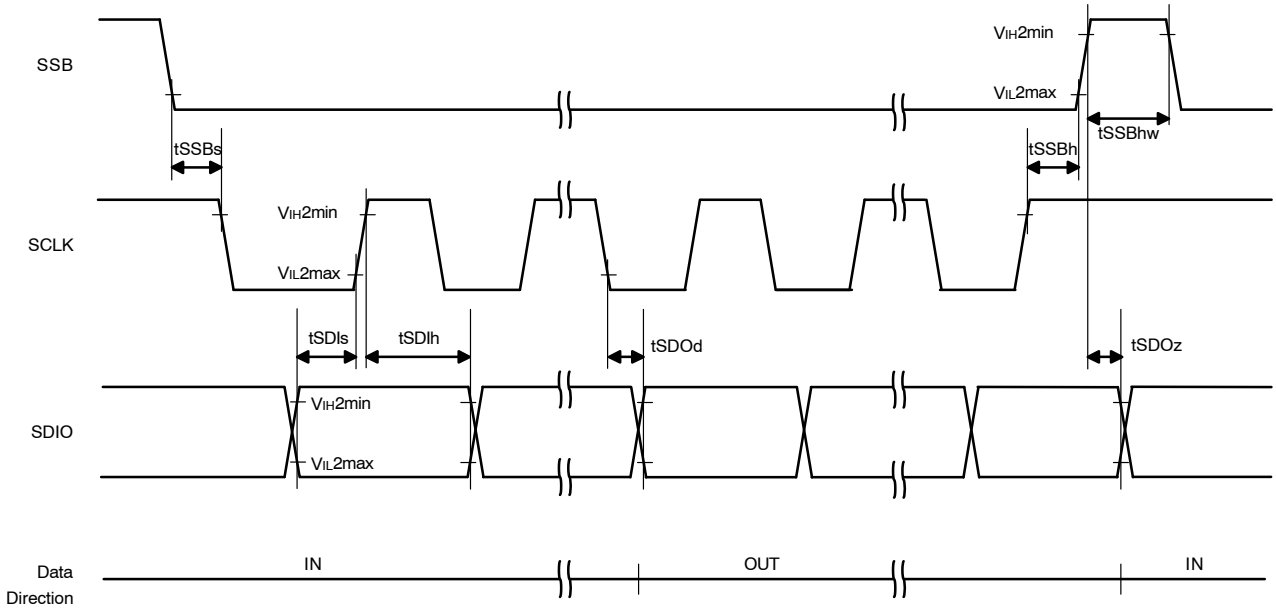


Figure 7. Digital Gyro Interface (Slave) Timing Definition

Table 11. DIGITAL GYRO INTERFACE(SLAVE) AC CHARACTERISTICS

Symbol	Item	Pin Name	Min	Typ	Max	Unit
FSCLK	SCLK Clock Frequency	SCLK	–	–	10	MHz
fSCLKdu	SCLK Duty	SCLK	30	–	70	%
tSSBhw	SSB High Period	SSB	100	–	–	ns
tSSBs	Setup Time for SCLK (F) of SSB	SSB SCLK	10	–	–	ns
tSSBh	Hold Time for SCLK (R) of SSB	SCLK SSB	10	–	–	ns
tSDIs	Setup Time for SCLK (R) of SDIO	SCLK SDIO	10	–	–	ns
tSDIh	Hold Time for SCLK (R) of SDIO	SCLK SDIO	10	–	–	ns
tSDOd	Delay Time from SCLK (F) to SDIO Update	SCLK SDIO	–	–	20	ns
tSDOz	Delay Time from SSB (R) to SDIO Invalid	SSB SDIO	–	–	20	ns
Cld	Load Capacitance	all	–	–	10	pF

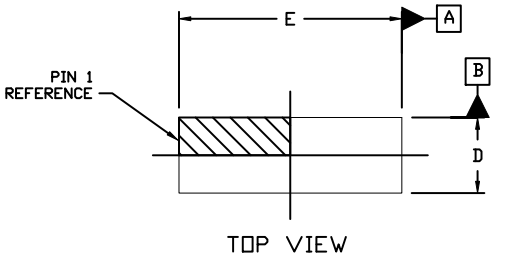
ORDERING INFORMATION

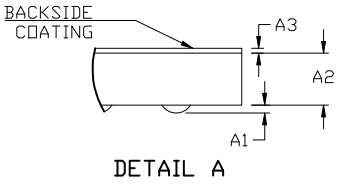
Device	Package Type	Shipping†
LC898262XHTBG	WLCSP10 0.77x2.27x0.33 (Pb−Free)	4000 / Tape & Reel

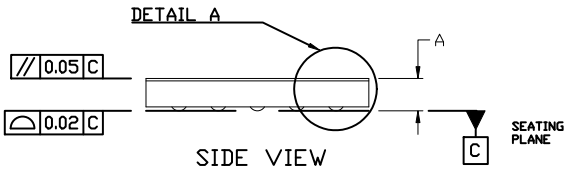
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

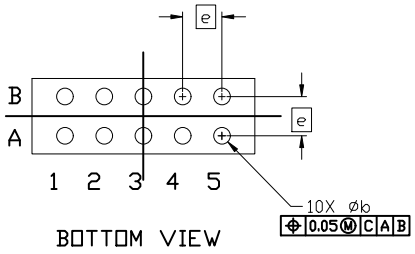
WLCSP10 0.77x2.27x0.33
CASE 567YK
ISSUE A

DATE 14 SEP 2020





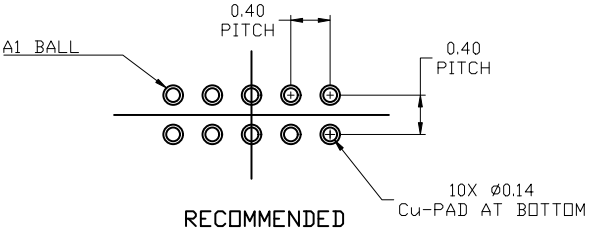




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

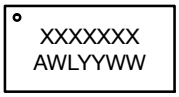
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.31	0.33	0.35
A1	0.034	0.040	0.046
A2	0.2525	0.265	0.2775
A3	0.025 REF		
b	0.15	0.17	0.19
D	0.720	0.770	0.820
E	2.220	2.270	2.320
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP10 0.77x2.27x0.33**		**PAGE 1 OF 1**

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