NCP4303A, NCP4303B

Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

The NCP4303A/B is a full featured controller and driver tailored to control synchronous rectification circuitry in switch mode power supplies. Thanks to its versatility, it can be used in various topologies such as flyback, forward and Half Bridge Resonant LLC.

The combination of externally adjustable minimum on and off times helps to fight the ringing induced by the PCB layout and other parasitic elements. Therefore, a reliable and noise less operation of the SR system is insured.

The extremely low turn off delay time, high sink current capability of the driver and automatic package parasitic inductance compensation system allow to maximize synchronous rectification MOSFET conduction time that enables further increase of SMPS efficiency.

Finally, a wide operating V_{CC} range combined with two versions of driver voltage clamp eases implementation of the SR system in 24 V output applications.

Features

- Self-Contained Control of Synchronous Rectifier in CCM, DCM, and QR Flyback Applications
- Precise True Secondary Zero Current Detection with Adjustable Threshold
- Automatic Parasitic Inductance Compensation Input
- Typically 40 ns Turn off Delay from Current Sense Input to Driver
- Zero Current Detection Pin Capability up to 200 V
- Optional Ultrafast Trigger Interface for Further Improved Performance in Applications that Work in Deep CCM
- Disable Input to Enter Standby or Low Consumption Mode
- Adjustable Minimum On Time Independent of V_{CC} Level
- Adjustable Minimum Off Time Independent of V_{CC} Level
- 5 A/2.5 A Peak Current Sink/Source Drive Capability
- Operating Voltage Range up to 30 V
- Gate Drive Clamp of Either 12 V (NCP4303A) or 6 V (NCP4303B)
- Low Startup and Standby Current Consumption
- Maximum Frequency of Operation up to 500 kHz
- SOIC−8 Package
- These are Pb-Free Devices

Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies
- Gaming Consoles
- All SMPS with High Efficiency Requirements

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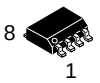
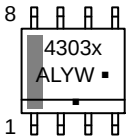
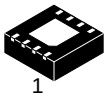
MARKING DIAGRAM



SOIC−8
D SUFFIX
CASE 751



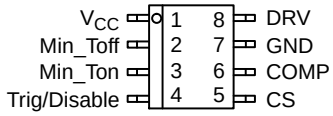


DFN8
CASE 488AF

4303x	= Specific Device Code x = A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT INFORMATION



(NOTE: For DFN the exposed pad must be either unconnected or preferably connected to ground. The GND pin must be always connected to ground.)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4303ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4303BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4303AMNTWG	DFN8 (Pb−Free)	4000 / Tape & Reel
NCP4303BMNTWG	DFN8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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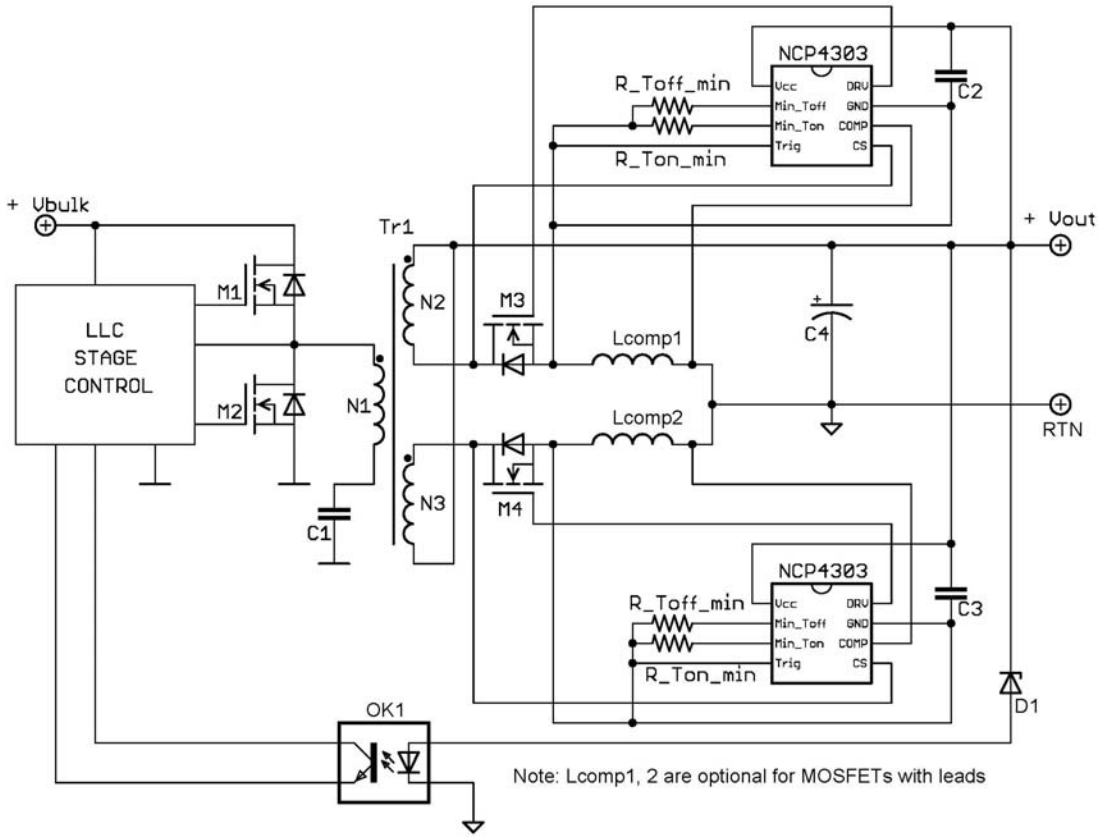


Figure 1. Typical Application Example – LLC Converter

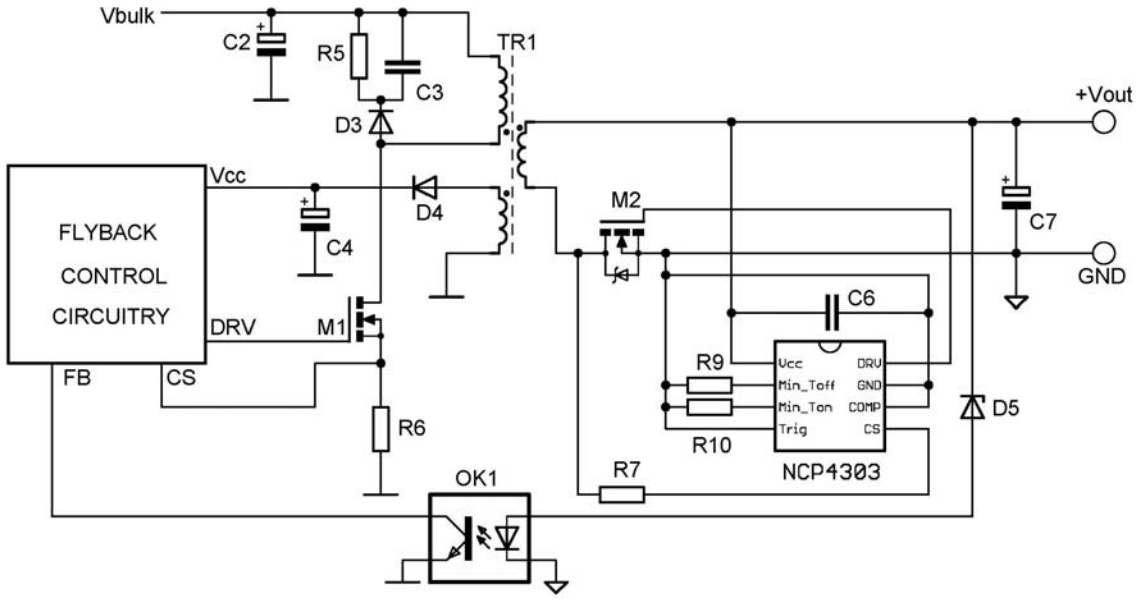


Figure 2. Typical Application Example − DCM, QR or CCM Flyback Converter

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	VCC	Supplies the driver	V_{CC} supply terminal of the controller. Accepts up to 30 V continuously.
2	Min_toff	Minimum off time adjust	Adjust the minimum off time period by connecting resistor to ground.
3	Min_ton	Minimum on time adjust	Adjust the minimum on time period by connecting resistor to ground.
4	TRIG/Disable	Forced reset input	This ultrafast turn-off input offers the possibility to further improve efficiency and performance in applications that work in deep Continuous Conduction Mode (CCM). Activates sleep mode if pulled up for more than 100 μs. Connect this pin to GND when not used.
5	CS	Current sense of the SR MOSFET	This pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn off detection threshold is 0 mV. A resistor in series with this pin can modify the turn off threshold if needed.
6	COMP	Compensation inductance connection	Use as a Kelvin connection to auxiliary compensation inductance. If SR MOSFET package parasitic inductance compensation is not used (like for SMT MOSFETs), connect this pin directly to GND pin.
7	GND	IC ground	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum ton, toff adjust resistors and trigger input. GND pin should be wired directly to the SR MOSFET source terminal/soldering point using Kelvin connection.
8	DRV	Gate driver output	Driver output for the SR MOSFET.

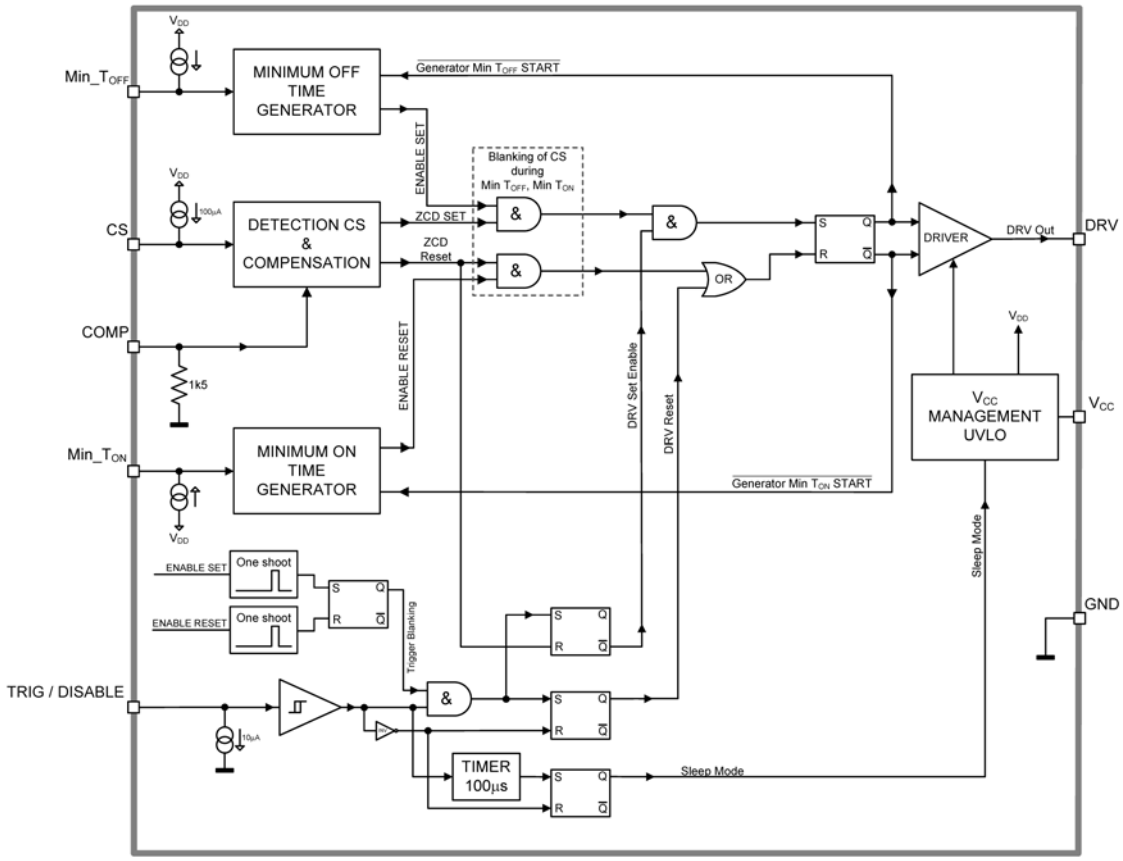


Figure 3. Internal Circuit Architecture

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	IC supply voltage	−0.3 to 30	V
V_{DRV}	Driver output voltage	−0.3 to 17	V
V_{CS}	Current sense input dc voltage	−4 to 200	V
V_{Csdyn}	Current sense input dynamic voltage (t_{pw} = 200 ns)	−10 to 200	V
V_{TRIG}	Trigger input voltage	−0.3 to 10	V
V_{Min_ton}, V_{Min_toff}	Min_Ton and Min_Toff input voltage	−0.3 to 10	V
$I_{_Min_Toff}$, $I_{_Min_Toff}$	Min_Ton and Min_Toff current	−10 to +10	mA
VGND−COMP	Static voltage difference between GND and COMP pins (internally clamped)	−3 to 10	V
VGND−COMP_dyn	Dynamic voltage difference between GND and COMP pins (t_{pw} = 200 ns)	−10 to 10	V
ICOMP	Current into COMP pin	−5 to 5	mA
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, SOIC version, A/B version	180	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, DFN − A/B versions, 50 mm^2 − 1.0 oz. Copper spreader	180	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, DFN − A/B versions, 600 mm^2 − 1.0 oz. Copper spreader	80	°C/W
T_{Jmax}	Maximum junction temperature	150	°C
T_{Smax}	Storage Temperature Range	−60 to +150	°C
T_{Lmax}	Lead temperature (Soldering, 10 s)	300	°C
	ESD Capability, Human Body Model except pin V_{CS} – pin 5, HBM ESD Capability on pin 5 is 650 V	2	kV
	ESD Capability, Machine Model	200	V
	ESD Capability, Charged Device Model	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1 − 8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
   Charged Device Model 250 V per JEDEC Standard JESD22−C101E.
2. This device meets latchup tests defined by JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, C_{load} = 0 nF, $R_{_min_ton}$ = $R_{_min_toff}$ = 10 kΩ, V_{trig} = 0 V, f_CS = 100 kHz, DC_CS = 50%, V_{CS_high} = 4 V, V_{CS_low} = −1 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC_on}	Turn−on threshold level (V_{CC} going up)	1	9.3	9.9	10.5	V
V_{CC_off}	Minimum operating voltage after turn−on (V_{CC} going down)	1	8.3	8.9	9.5	V
V_{CC_hyste}	V_{CC} hysteresis	1	0.8	1.0	1.3	V
I_{CC1_A} I_{CC1_B}	Internal IC consumption (no output load on pin 8, F_{sw} = 500 kHz, R_{Ton_min} = R_{Toff_min} = 5 kΩ)	1	− −	4.7 4	− −	mA
I_{CC2_A} I_{CC2_B}	Internal IC consumption (C_{load} = 1 nF on pin 8, F_{sw} = 400 kHz, R_{Ton_min} = R_{Toff_min} = 5 kΩ)	1	− −	9.3 6.4	− −	mA
I_{CC3_A} I_{CC3_B}	Internal IC consumption (C_{load} = 10 nF on pin 8, F_{sw} = 400 kHz, R_{Ton_min} = R_{Toff_min} = 5 kΩ)	1	− −	54 34	− −	mA
I_{CC_SDM}	Startup current consumption (V_{CC} = $V_{CC_}$on − 0.1 V) and consumption during light load (disable) mode, (F_{sw} = 500 kHz, V_{trig} = 5 V)	1	−	390	550	μA
$I_{CC_SDM\ NS}$	Startup current consumption (V_{CC} = $V_{CC_}$on − 0.1 V) and consumption during light load (disable) mode, (V_{cs} = 0 V, V_{trig} = 5 V)	1	−	280	450	μA
DRIVE OUTPUT						
t_{r_A}	Output voltage rise−time for A version (C_{load} = 10 nF), (Note 3)	8	−	120	−	ns
t_{r_B}	Output voltage rise−time for B version (C_{load} = 10 nF), (Note 3)	8	−	80	−	ns
t_{f_A}	Output voltage fall−time for A version (C_{load} = 10 nF), (Note 3)	8	−	50	−	ns
t_{f_B}	Output voltage fall−time for B version (C_{load} = 10 nF), (Note 3)	8	−	35	−	ns
R_{oh}	Driver source resistance (Note 3)	8	−	1.8	7	Ω
R_{ol}	Driver sink resistance	8	−	1	2	Ω
$I_{DRV_pk(source)}$	Output source peak current (Note 3)	8	−	2.5	−	A
$I_{DRV_pk(sink)}$	Output sink peak current (Note 3)	8	−	5	−	A
$V_{DRV(H)_A}$	Driver high level output voltage on A version (C_{load} = 1 nF)	8	10	−	−	V
$V_{DRV(H)_A}$	Driver high level output voltage on A version (C_{load} = 10 nF)	8	11.8	−	−	V
$V_{DRV(H)_B}$	Driver high level output voltage on B version (C_{load} = 1 nF)	8	5	−	−	V
$V_{DRV(H)_B}$	Driver high level output voltage on B version (C_{load} = 10 nF)	8	6	−	−	V
$V_{DRV(min_A)}$	Minimum drive output voltage for A version (V_{CC} = V_{CC_off} + 200 mV)	8	8.3	−	−	V
$V_{DRV(min_B)}$	Minimum drive output voltage for B version (V_{CC} = V_{CC_off} + 200 mV)	8	4.5	−	−	V
$V_{DRV(CLMP_A)}$	Driver clamp voltage for A version, (12 V < V_{CC} < 28 V, minimum C_{load} = 1 nF)	8	−	12	16	V
$V_{DRV(CLMP_B)}$	Driver clamp voltage for B version, (12 V < V_{CC} < 28 V, minimum C_{load} = 1 nF)	8	−	7	8.3	V
CS INPUT						
T_{pd_on}	The total propagation delay from CS input to DRV output turn on (V_{CS} goes down from 4 V to −1 V, t_{f_CS} = 5 ns, COMP pin connected to GND)	5, 8	−	60	90	ns
T_{pd_off}	The total propagation delay from CS input to DRV output turn off (V_{CS} goes up from −1 V to 4 V, t_{r_CS} = 5 ns, COMP pin connected to GND), (Note 3)	5, 8	−	40	55	ns
I_{shift_CS}	Current sense input current source (V_{CS} = 0 V)	5	95	100	105	μA
$V_{th_cs_on}$	Turn on current sense input threshold voltage	5, 8	−120	−85	−50	mV
$V_{th_cs_off}$	Current sense pin turn off threshold voltage, COMP pin connected to GND (Note 3)	5, 8	−1	−	0	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, C_{load} = 0 nF, $R_{_min_ton}$ = $R_{_min_toff}$ = 10 kΩ, V_{trig} = 0 V, f_CS = 100 kHz, DC_CS = 50%, V_{CS_high} = 4 V, V_{CS_low} = −1 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CS INPUT						
G_{comp}	Compensation inverter gain (Note 3)	5,6,8	−	−1	−	−
$I_{CS_Leakage}$	CS input leakage current, V_{CS} = 200 Vdc	5	−	−	1	μA
TRIGGER/DISABLE INPUT						
T_{trig_pw}	Minimum trigger pulse duration	4	30	−	−	ns
V_{trig}	Trigger input threshold voltage (V_{trig} goes up)	4	1.5	−	2.5	V
t_{p_trig}	Propagation delay from trigger input to the DRV output (V_{trig} goes up from 0 to 5 V t_{r_trig} = 5 ns)	4	−	−	30	ns
$t_{trig_light_load}$	Light load turn off filter duration	4	−	100	−	μs
$t_{trig_light_load_rec}$	IC operation recovery time when leaving light load disable mode (V_{trig} goes down from 5 to 0 V t_{f_trig} = 5 ns)	4	−	−	550	ns
I_{trig}	Trigger input pull down current (V_{trig} = 5 V)	4	−	10	−	uA
MINIMUM T_{on} AND T_{off} ADJUST						
T_{on_min}	Minimum T_{on} period ($R_{T_on_min}$ = 0 Ω)	3	−	300	−	ns
T_{off_min}	Minimum T_{off} period ($R_{T_off_min}$ = 0 Ω)	2	−	620	−	ns
T_{on_min}	Minimum T_{on} period ($R_{T_on_min}$ = 10 kΩ)	3	0.9	1.0	1.1	μs
T_{off_min}	Minimum T_{off} period ($R_{T_off_min}$ = 10 kΩ)	2	0.9	1.0	1.1	μs
T_{on_min}	Minimum T_{on} period ($R_{T_on_min}$ = 50 kΩ)	3	−	4.8	−	μs
T_{off_min}	Minimum T_{off} period ($R_{T_off_min}$ = 50 kΩ)	2	−	4.8	−	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design.

TYPICAL CHARACTERISTICS

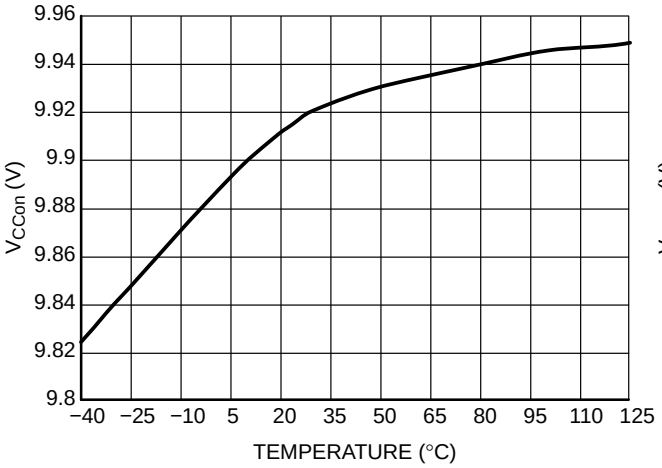


Figure 4. V_{CC} Startup Voltage

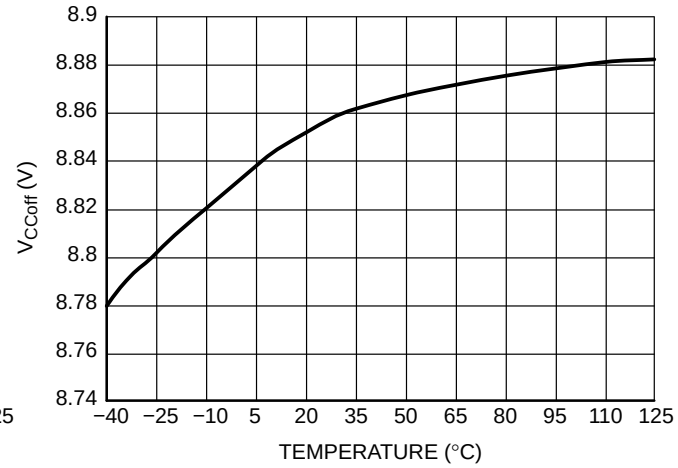


Figure 5. V_{CC} Turn−off Voltage

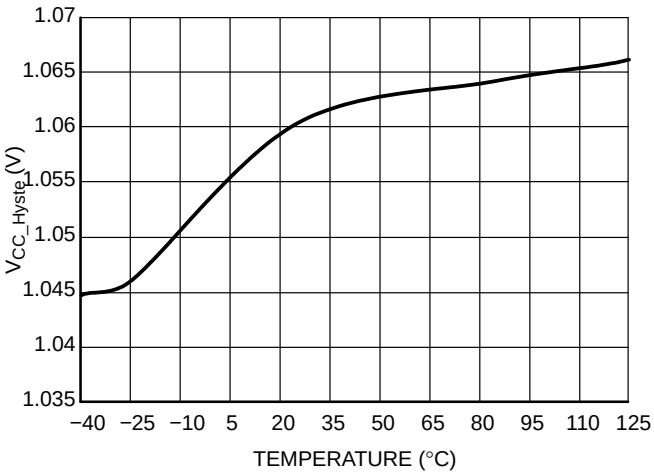


Figure 6. V_{CC} Hysteresis

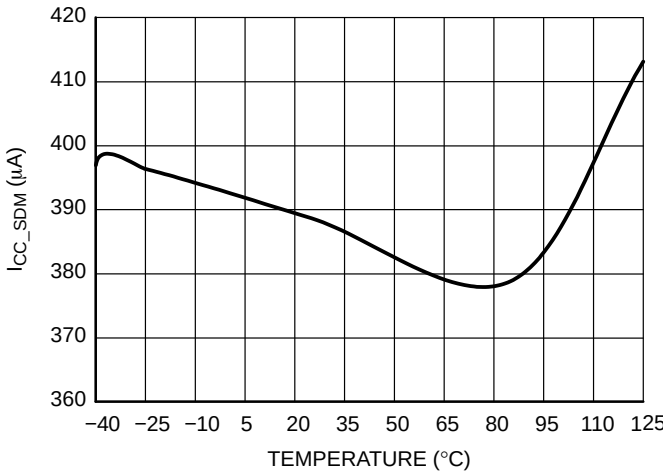


Figure 7. Startup Current

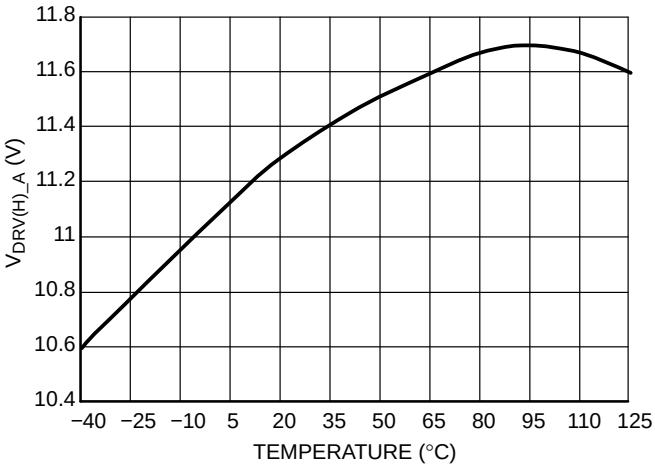


Figure 8. Driver High Level – A Version, V_{CC} = 12 V and C_{load} = 1 nF

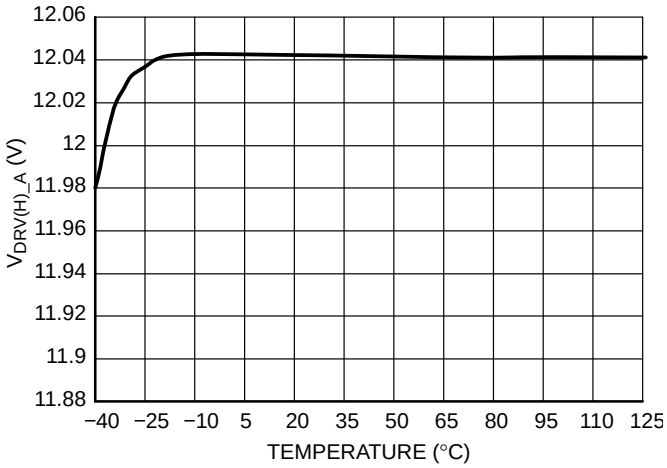


Figure 9. Driver High Level− A Version, V_{CC} = 12 V and C_{load} = 10 nF

TYPICAL CHARACTERISTICS

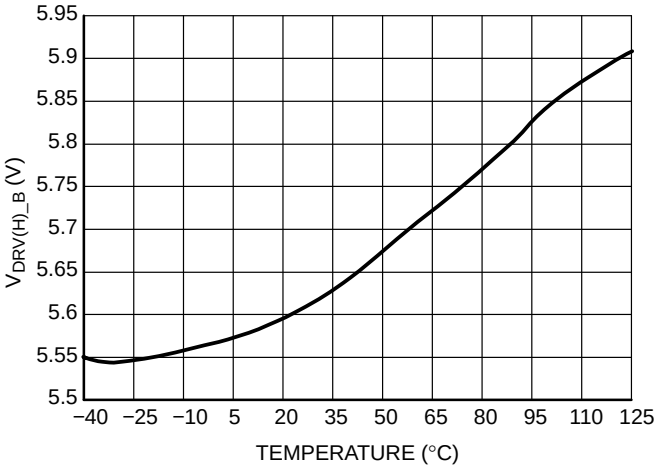


Figure 10. Driver High Level – B Version, V_{CC} = 12 V and C_{load} = 1 nF

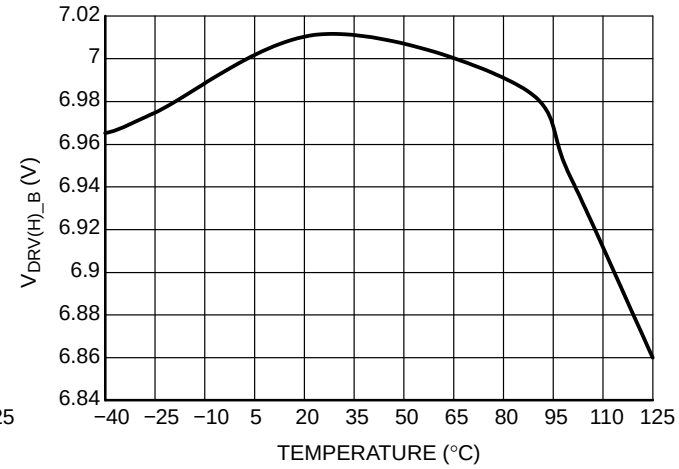


Figure 11. Driver High Level – B Version, V_{CC} = 12 V and C_{load} = 10 nF

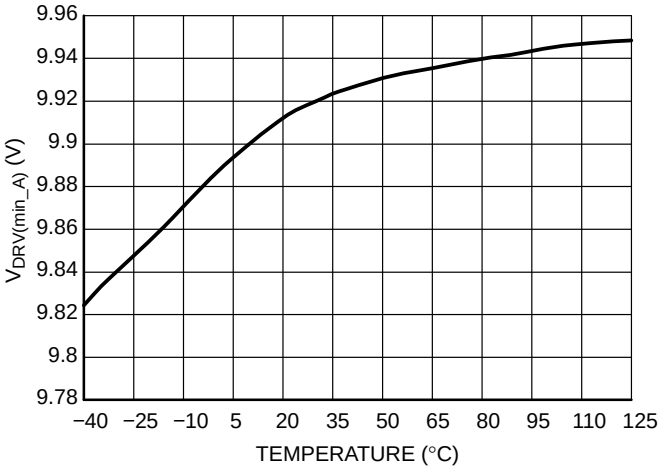


Figure 12. Minimal Driver High Level – A Version, V_{CC} = V_{CC_OFF} + 0.2 V and C_{load} = 0 nF

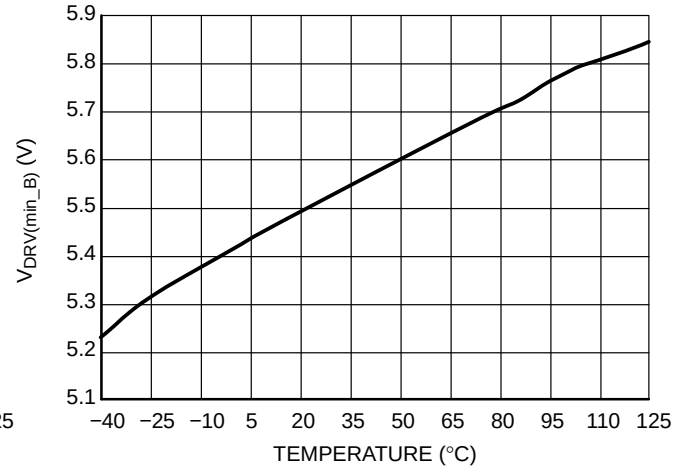


Figure 13. Minimal Driver High Level – B Version, V_{CC} = V_{CC_OFF} + 0.2 V and C_{load} = 0 nF

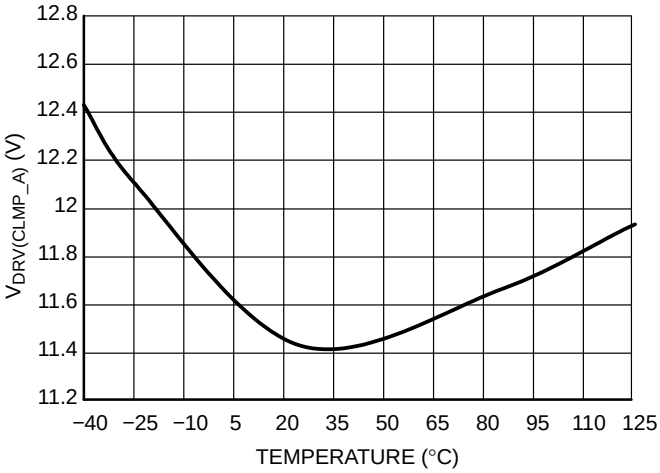


Figure 14. Driver Clamp Level – A Version, V_{CC} = 28 V and C_{load} = 1 nF

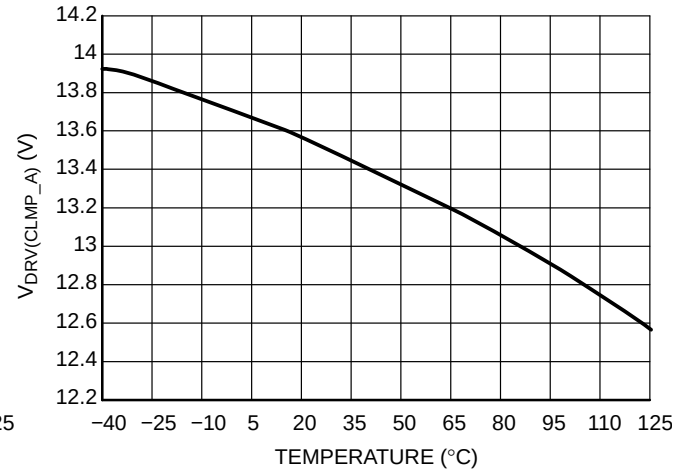


Figure 15. Driver Clamp Level – A Version, V_{CC} = 28 V and C_{load} = 10 nF

TYPICAL CHARACTERISTICS

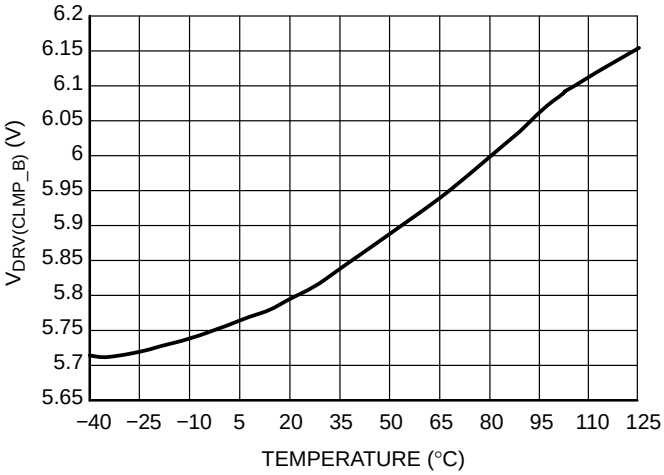


Figure 16. Driver Clamp Level – B Version, V_{CC} = 28 V and C_{load} = 1 nF

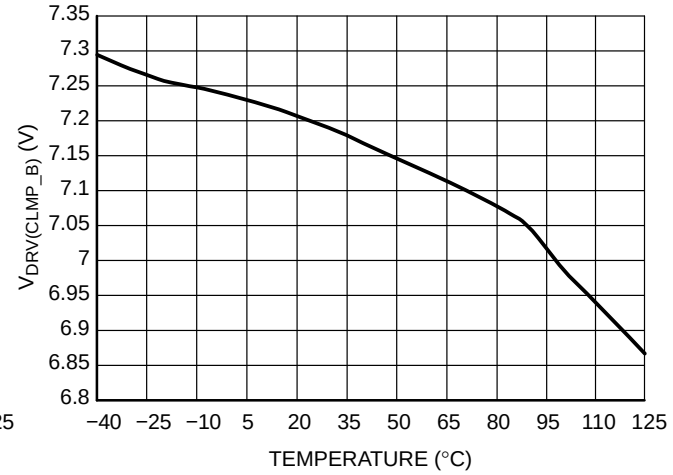


Figure 17. Driver Clamp Level – B Version, V_{CC} = 28 V and C_{load} = 10 nF

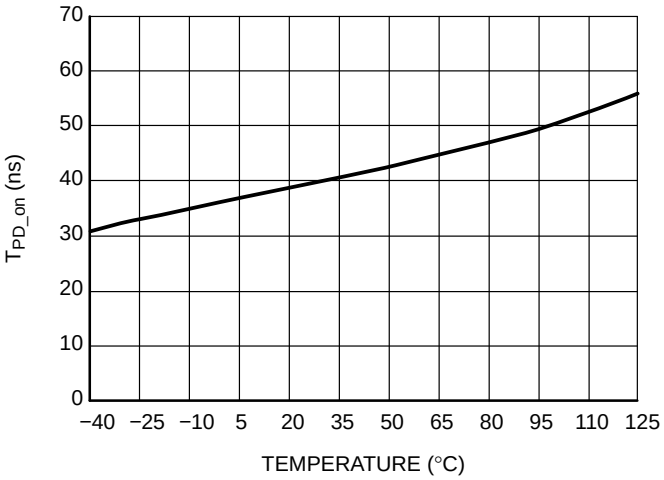


Figure 18. CS to DRV Turn−on Propagation Delay

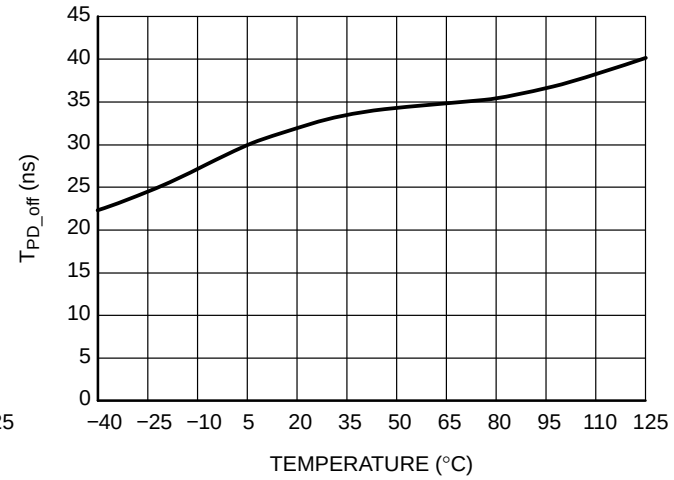


Figure 19. CS to DRV Turn−off Propagation Delay

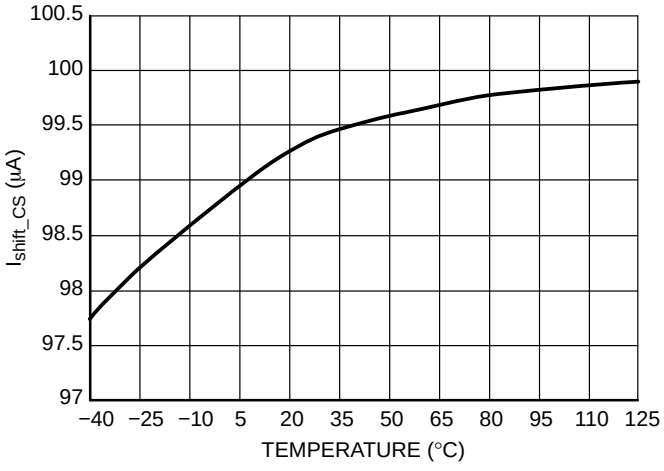


Figure 20. CS Pin Shift Current

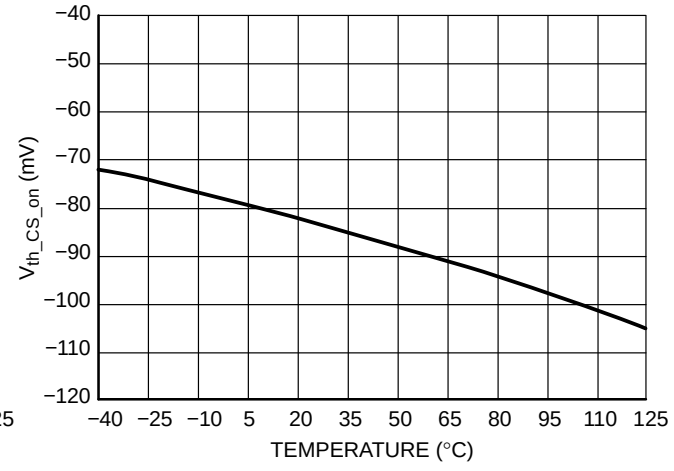


Figure 21. CS Turn−on Threshold

TYPICAL CHARACTERISTICS

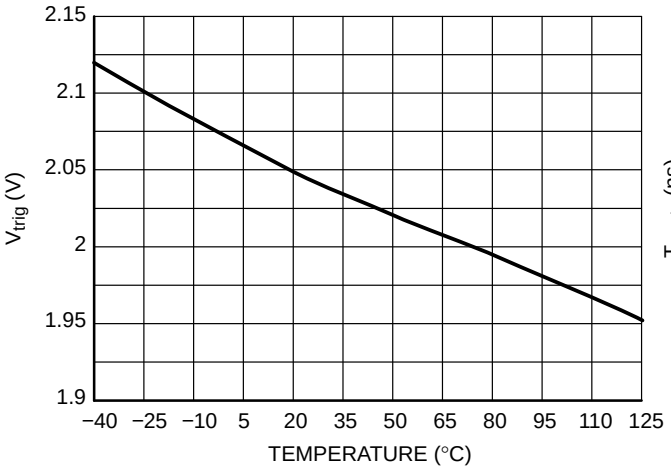


Figure 22. Trigger Input Threshold Voltage

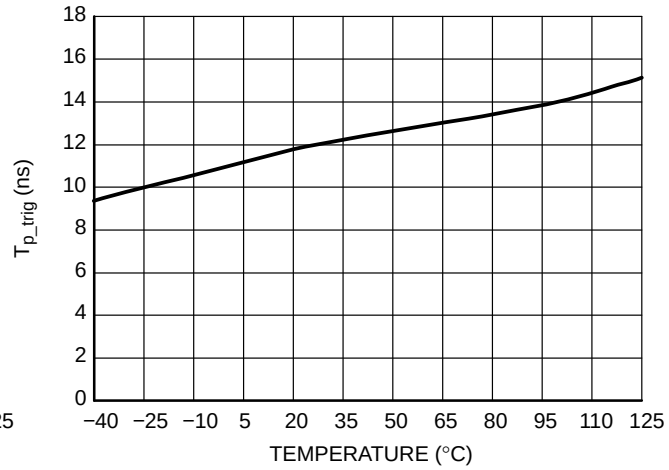


Figure 23. Propagation Delay from Trigger Input to DRV Turn−off

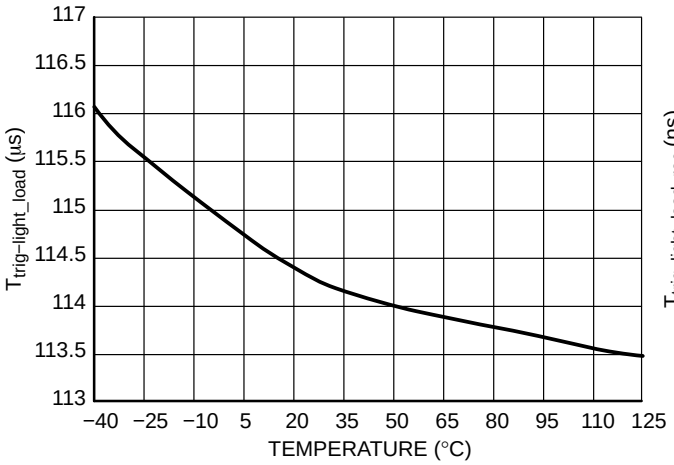


Figure 24. Light Load Transition Timer Duration

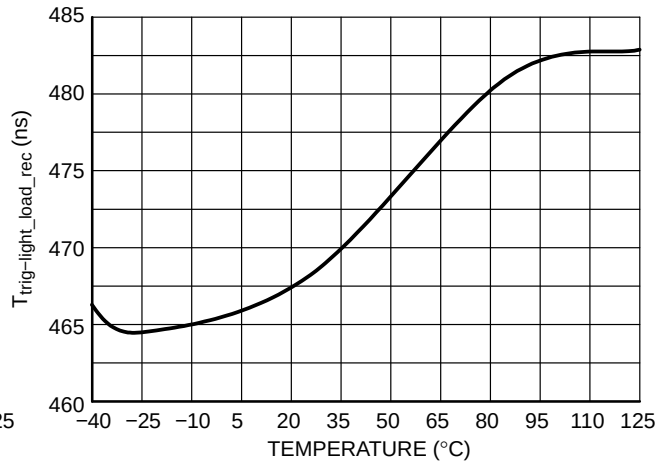


Figure 25. Light Load to Normal Operation Recovery Time

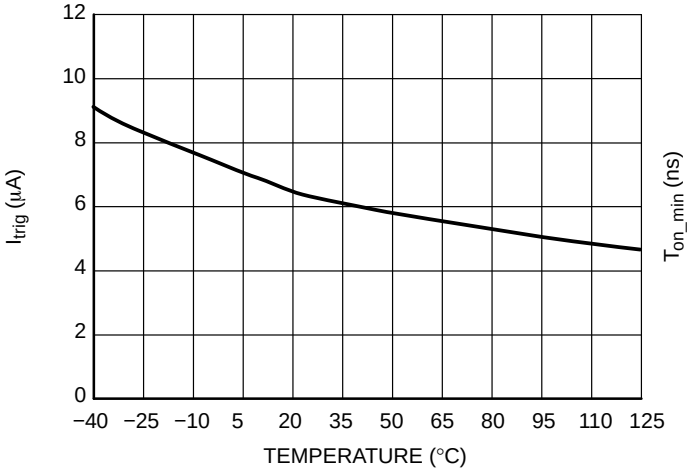


Figure 26. Trigger Input Pulldown Current

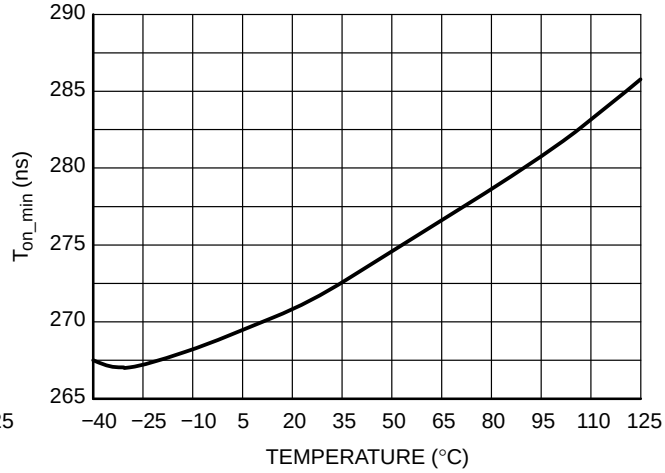


Figure 27. Minimum on Time @ $R_{t_on_min}$ = 0 Ω

TYPICAL CHARACTERISTICS

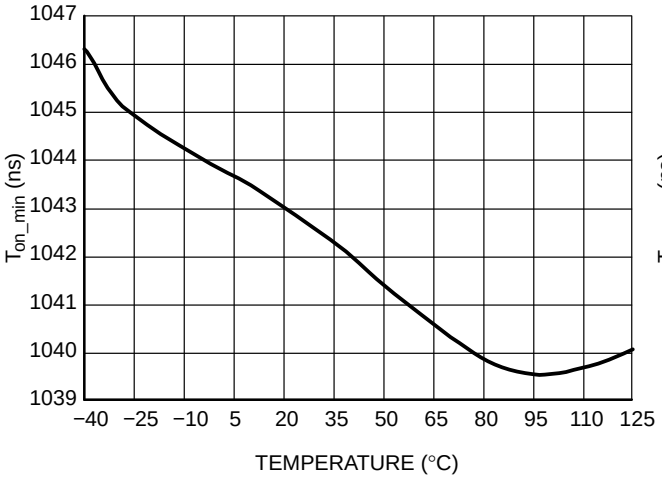


Figure 28. Minimum on Time @ $R_{t_on_min}$ = 10 kΩ

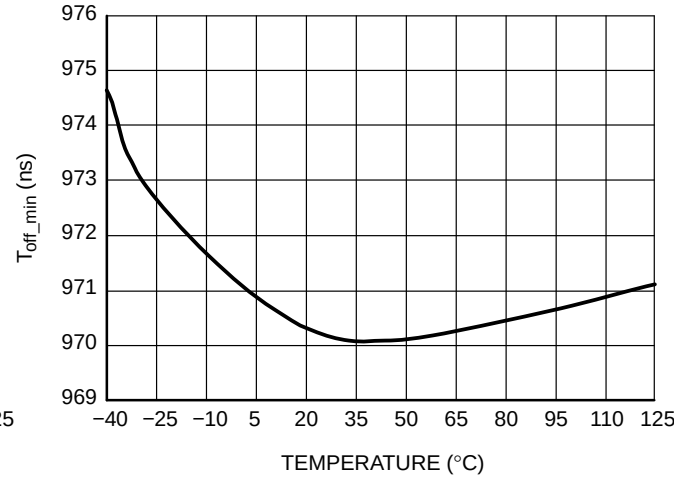


Figure 29. Minimum Off Time @ $R_{t_off_min}$ = 10 kΩ

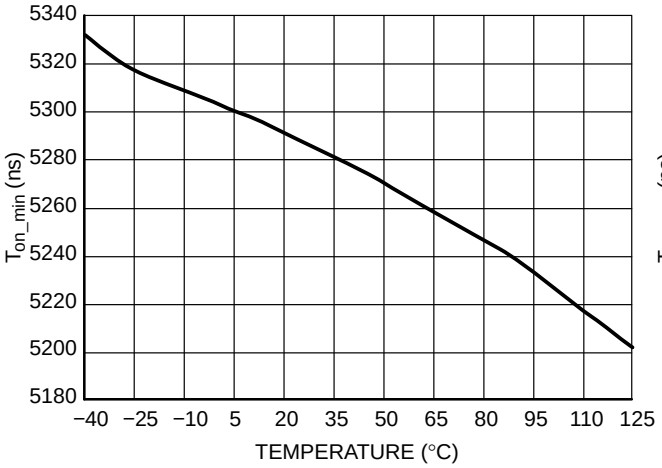


Figure 30. Minimum on Time @ $R_{t_on_min}$ = 53 kΩ

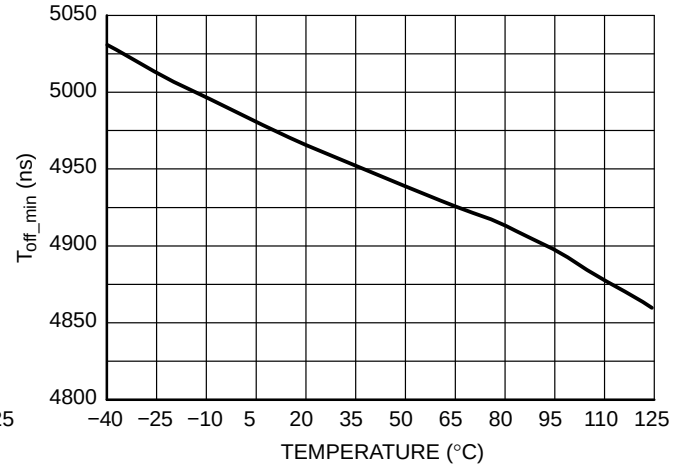


Figure 31. Minimum Off Time @ $R_{t_off_min}$ = 53 kΩ

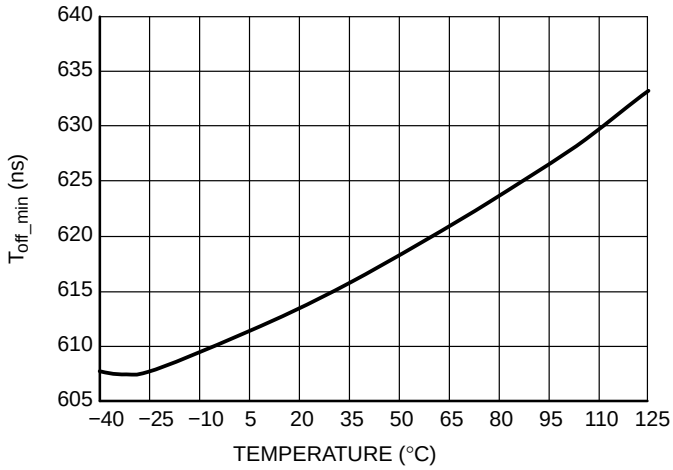


Figure 32. Minimum Off Time @ $R_{t_off_min}$ = 0 Ω

APPLICATION INFORMATION

General Description

The NCP4303 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4303 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4303 works from an available bias supply with voltage range from 10.4 V to 28 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebook and LCD TV adapters. As a result, the NCP4303 simplifies circuit operation compared to other devices that require specific bias power supply (e.g. 5 V). The high voltage capability of the V_{CC} pin is also a unique feature designed to allow operation for a broader range of applications.

Precise turn off threshold of the current sense comparator together with accurate offset current source allows the user to adjust for any required turn off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn off thresholds in the range of −10 mV to −5 mV, the NCP4303 offers a turn off threshold of 0 mV that in combination with a low $R_{DS(on)}$ SR MOSFET significantly reduces the turn off current threshold and improves efficiency.

To overcome issues after turn on and off events, the NCP4303 provides adjustable minimum on time and off time blanking periods. Blanking times can be adjusted independently of IC V_{CC} using resistors connected to GND. If needed, blanking periods can be modulated using additional components.

The NCP4303 ZCD comparator features very short turn-off delay time. This allows the SR controller to be used in applications operating in shallow CCM mode without any extra primary side synchronization circuitry (refer to Figures 2 and 60). This circuit exhibits excellent efficiency results (refer to Figures 58 and 59). A typical example of such an application is a flyback notebook adapter that usually enters only shallow CCM when Vbulk is lower than approximately 180 Vdc. On the other hand, the turn-off delay could be too long for applications operating in deep CCM (like high output current flyback or forward converters). High reverse current spikes and also drain voltage ringing are then usually present on the SR MOSFET. This is because the SR MOSFET needs some time to fully turn-off. The NCP4303 offers an optional ultrafast turn-off trigger input to prevent these current spikes and drain voltage ringing. This input can be used to turn-off the SR MOSFET earlier, using a synchronization signal from the primary side. The SR MOSFET is then turned-off prior to it's drain voltage reversing thus the reverse current is minimized while the efficiency is maximized (refer to Figure 46 for a deep CCM flyback converter example). Using the trigger input is optional and only recommended for applications operating in deep CCM. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS.

Finally, the NCP4303 features a special input that can be used to automatically compensate for SR MOSFET parasitic inductance effect. This technique achieves the maximum available on−time and thus optimizes efficiency when a MOSFET in standard package (like TO220 or TO247) is used. If a SR MOSFET in SMT package with negligible inductance is used, the compensation input is connected to GND pin.

Zero Current Detection and parasitic inductance compensation

Figure 33 shows the internal connection of the ZCD circuitry on the current sense input. The synchronous rectification MOSFET is depicted with it's parasitic inductances to demonstrate operation of the compensation system.

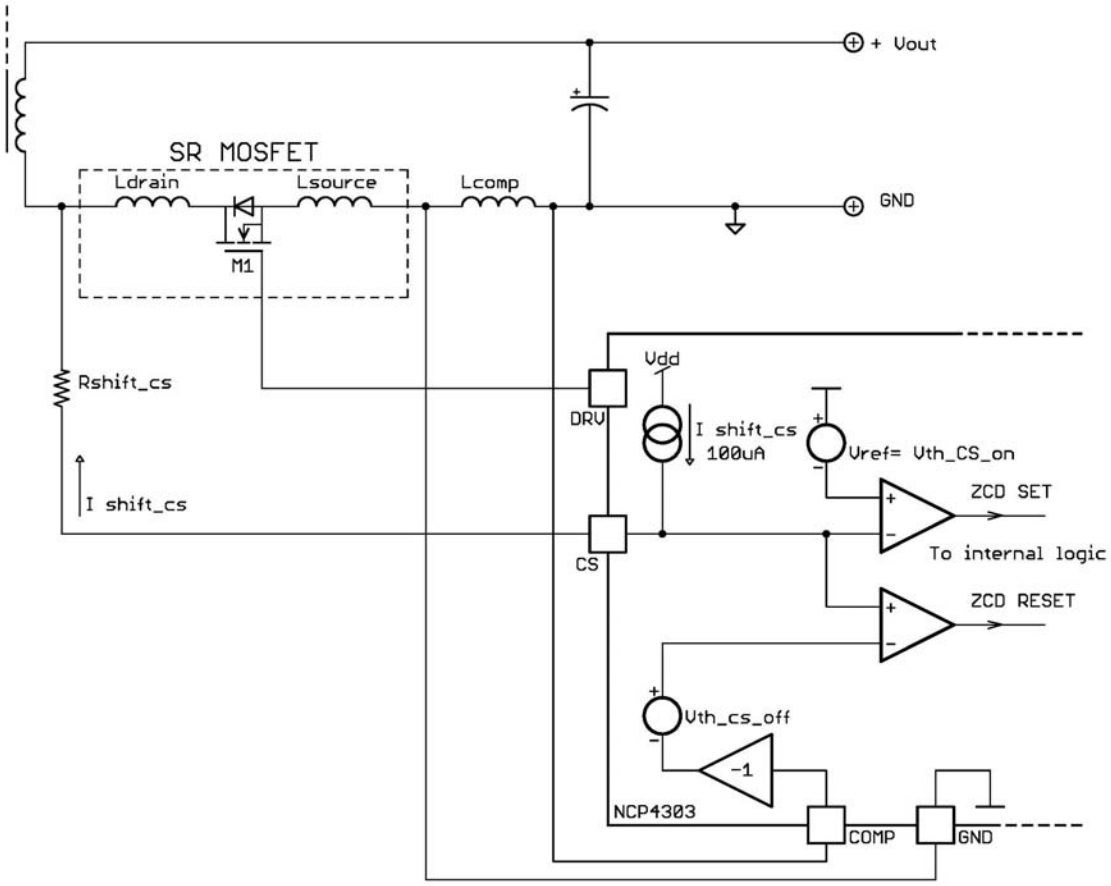


Figure 33. ZCD Sensing Circuitry Functionality

When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. The CS pin sources current of 100 μA that creates a voltage drop on the R_{shift_cs} resistor. Once the voltage on the CS pin is lower than $V_{th_cs_on}$ threshold, M1 is turned on. Because of parasitic impedances, significant ringing can occur in the application. To overcome sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using $R_{_Min_Ton}$ resistor.

The SR MOSFET is turned−off as soon as the voltage on the CS pin is higher than $V_{th_cs_off}$. For the same ringing reason, a minimum off time timer is asserted once the turn−off is detected. The minimum off time can be externally adjusted using $R_{_Min_Toff}$ resistor. MOSFET M1 channel conducts when the secondary current decreases, therefore the turn−off time depends on its $R_{DS(on)}$. The 0 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn off. The R_{shift_cs} resistor provides the designer with the possibility to modify (increase) the actual turn−off current threshold.

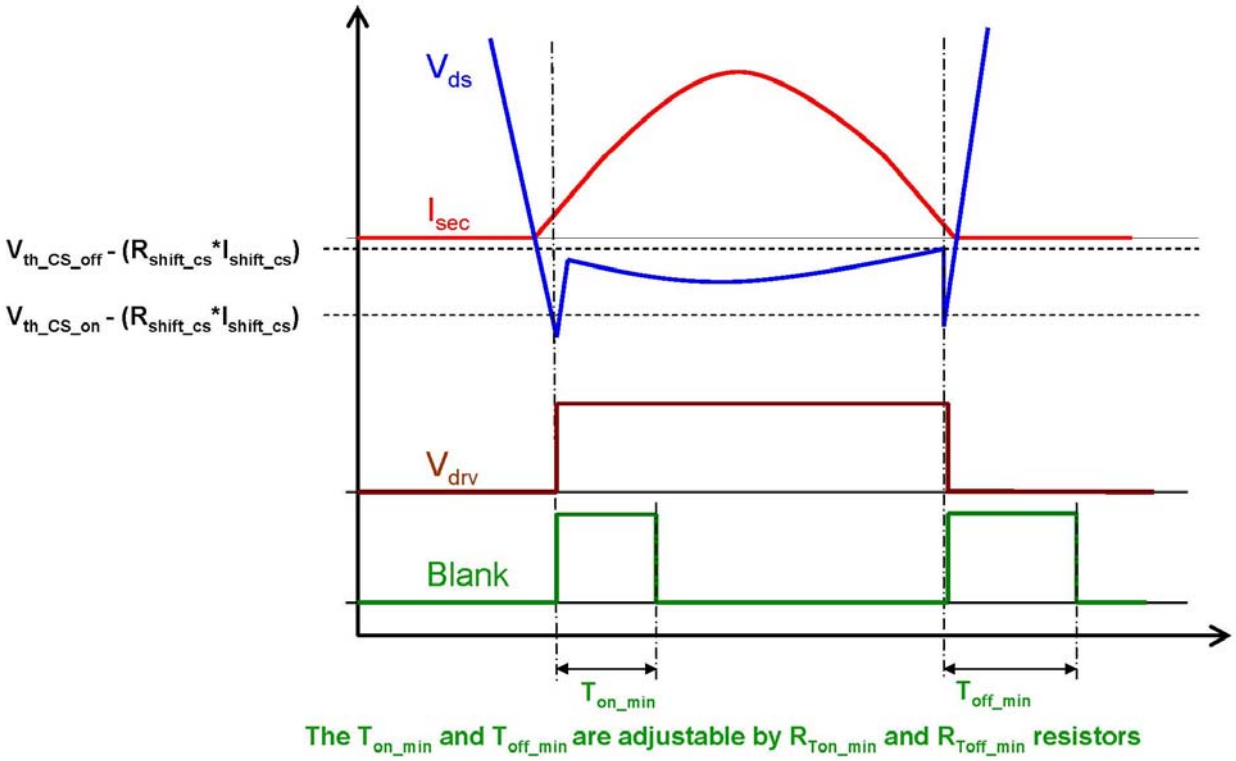


Figure 34. ZCD Comparators Thresholds and Blanking Periods Timing

If no R_{shift_cs} resistor is used, the turn−on and turn−off thresholds are fully given by the CS input specification (please refer to parametric table). Once non−zero R_{shift_cs} resistor is used, both thresholds move down (i.e. higher MOSFET turn off current) as the CS pin offset current causes a voltage drop that is equal to:

$$V_Rshift_cs = Rshift_cs * Ishift_cs \quad \text{(eq. 1)}$$

Final turn−on and turn off thresholds can be then calculated as:

$$VCS_turn_on = Vth_CS_on - (Rshift_cs * Ishift_cs) \quad \text{(eq. 2)}$$

$$VCS_turn_off = Vth_CS_off - (Rshift_cs * Ishift_cs) \quad \text{(eq. 3)}$$

Note that R_{shift_cs} impact on turn−on threshold is less critical compare to turn−off threshold.

If using a SR MOSFET in TO220 package (or other package which features leads), the parasitic inductance of the package leads causes a turn−off current threshold increase. This is because current that flows through the SR MOSFET has quite high di(t)/dt that induces error voltage on the SR MOSFET leads inductance. This error voltage, that is proportional to the secondary current derivative, shifts the CS input voltage to zero when significant current still flows through the channel. Zero current threshold is thus detected when current still flows through the SR MOSFET channel – please refer to Figure 35 for better understanding. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized.

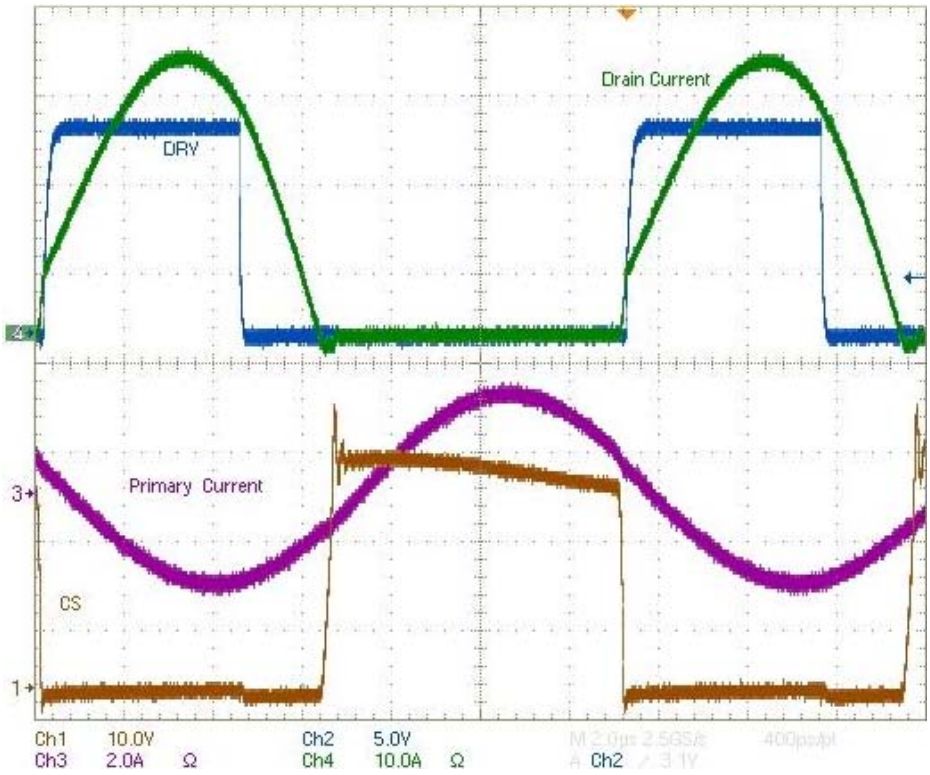


Figure 35. Waveforms from SR System Using MOSFET in TO220 Package without Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Reduced

Note that the efficiency impact of the error caused by parasitic inductance increases with lower $R_{DS(on)}$ MOSFETs and/or higher operating frequency.

The NCP4303 offers a way to compensate for MOSFET parasitic inductances effect − refer to Figure 36.

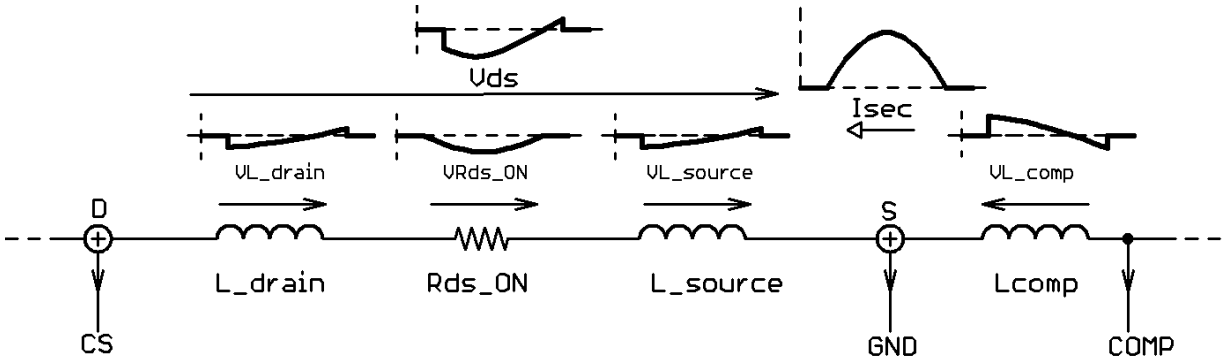


Figure 36. Package Parasitic Inductances Compensation Principle

Dedicated input (COMP) offers the possibility to use an external compensation inductance (wire strap or PCB). If the value of this compensation inductance is $L_{comp} = L_{drain} + L_{source}$, the compensation voltage created on this inductance is exactly the same as the sum of error voltages created on drain and source parasitic inductances i.e. $VL_{drain} + VL_{source}$. The internal analog inverter (Figure 33) inverts compensation voltage Vl_comp and offsets the current sense comparator turn−off threshold. The current sense comparator thus “sees” between its terminals a voltage that would be seen on the SR MOSFET channel resistance in case the lead inductances wouldn’t exist. The current sense comparator of the NCP4303 is thus able to detect the secondary current zero crossing very precisely. More over, the secondary current turn−off threshold is then di(t)/t independent thus the NCP4303 allows to increase operating frequency of the SR system. One should note that the parasitic resistance of compensation inductance should be as low as possible compared to the SR MOSFET channel and leads resistance otherwise compensation is not efficient.

Typical value of compensation inductance for a TO220 package is 7 nH. The parasitic inductance can differ depends on how much are the leads shortened during the assembly process. The compensation inductance design has to be done with enough margin to overcome situation that the system will become overcompensated due to packaging and assembly process variations. Waveforms from the application with compensated SR system can be seen in Figure 37. One can see the conduction time has been significantly increased and turn−off current reduced.

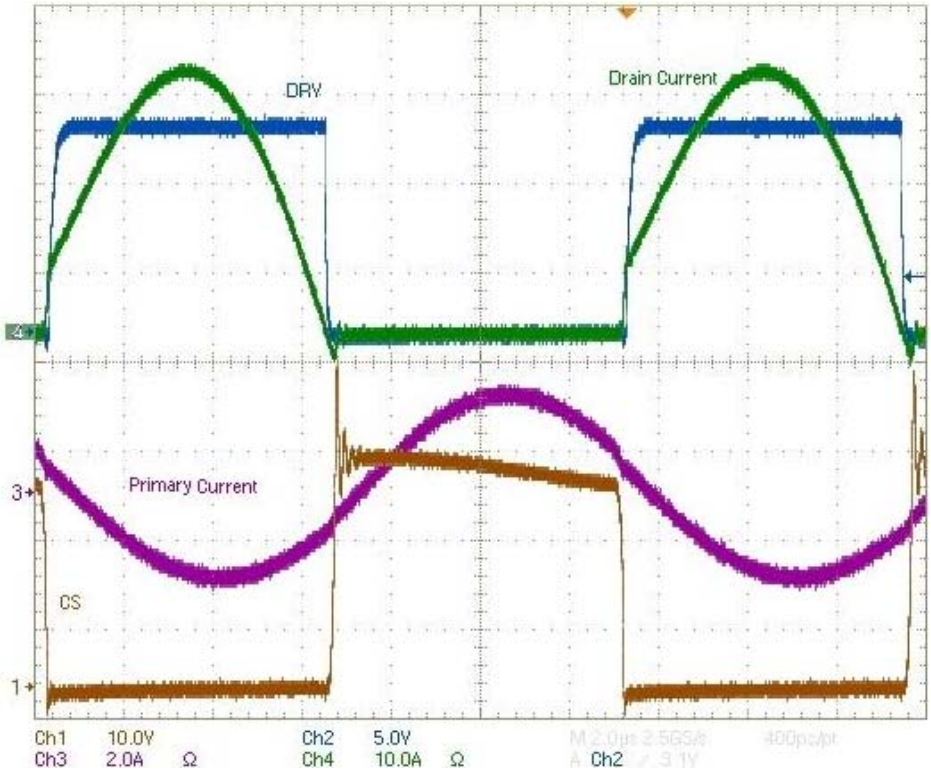


Figure 37. Waveforms from SR System Using MOSFET in TO220 Package with Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time Optimized

Note that using the compensation system is only beneficial in applications that are using a low $R_{DS(on)}$ MOSFET in non−SMT package. Using the compensation method allows for optimized efficiency with a standard TO220 package that in turn results in reduced costs, as the SMT MOSFETs usually require reflow soldering process and more expensive PCB.

From the above paragraphs and parameter tables it is evident that turn−off threshold precision is quite critical. If we consider a SR MOSFET with $R_{DS(on)}$ of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn−off current threshold difference. Thus the PCB layout is very critical when implementing the SR system. Note that the CS turn−off comparator as well as compensation inputs are referred to the GND pin. Any parasitic impedance (resistive or inductive − talking about mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. Practically this is not possible because of the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented (i.e. GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point). Any impact of PCB parasitic elements on the SR controller functionality is then avoided. Figures 38 and 39 show examples of SR system layouts using parasitic inductance compensation (i.e. for low $R_{DS(on)}$ MOSFET in TO220 package) and not using compensation (i.e. for higher $R_{DS(on)}$ MOSFET in TO220 package or SMT package MOSFETs).

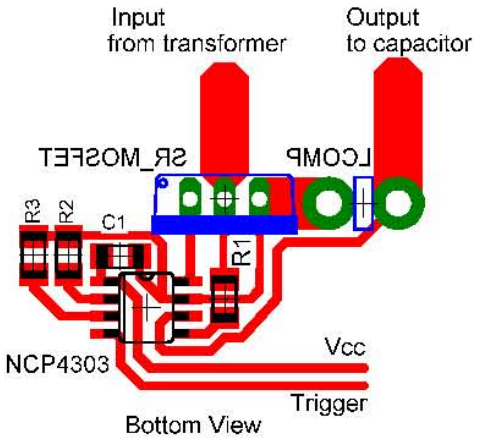


Figure 38. Recommended Layout for SO8 Package When Parasitic Inductance Compensation is Used

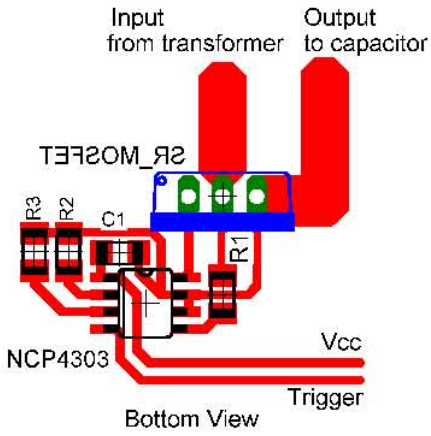


Figure 39. Recommended Layout for SO8 Package When Parasitic Inductance Compensation is Not Used

Trigger/Disable input

The NCP4303 features an ultrafast trigger input that exhibits a typically of 12 ns delay from its activation to the turn−off of the SR MOSFET. This input offers a possibility to turn−off the SR MOSFET in applications that operates in deep CCM via a signal coming from the primary side. Efficiency and SR performance can be thus further optimized (refer also to application information on page 12). The primary trigger signal rising edge should come to the trigger input before the secondary voltage reverses. Thus the driver signal for primary switch should be delayed – refer to figure 46 for one possible method of delaying the primary driving signal in CCM flyback topology. The trigger signal is disabled from the end of the minimum off time period to the end of the minimum on time period. This technique is used to:

a) Overcome false turn−off of the gate driver in case the synchronization pulse is too wide and comes twice per switching period (in HB and HB LLC applications).

b) Increase trigger input noise immunity against the parasitic ringing that is present in the SMPS layout during the turn on process.

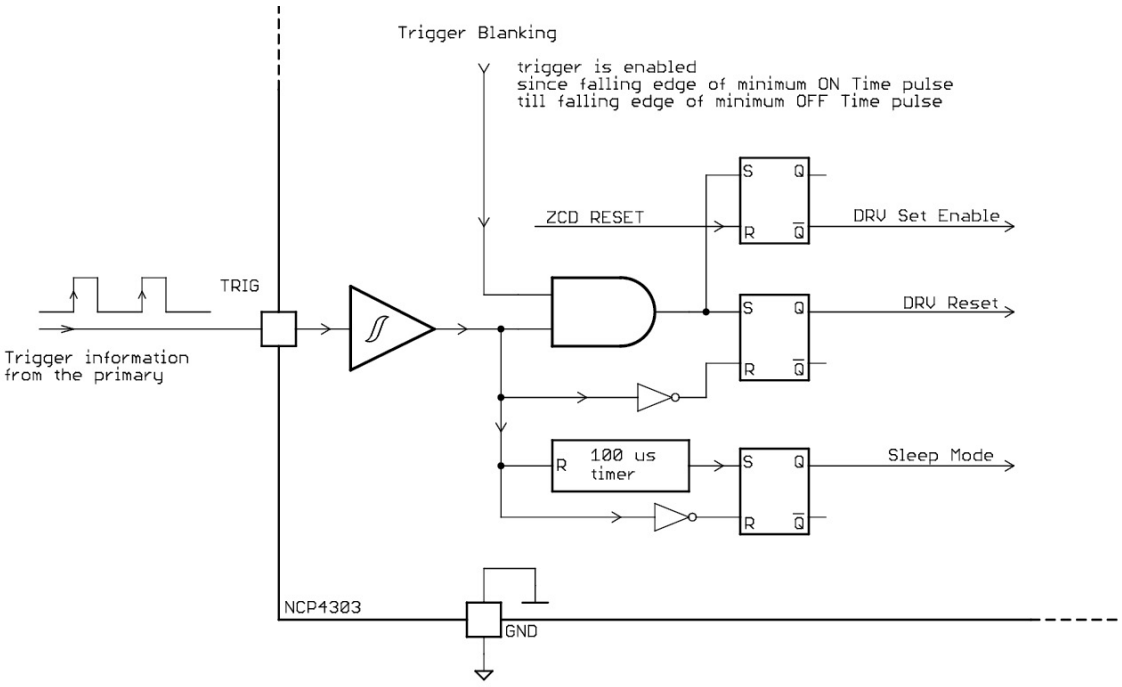


Figure 40. Trigger Input Internal Connection

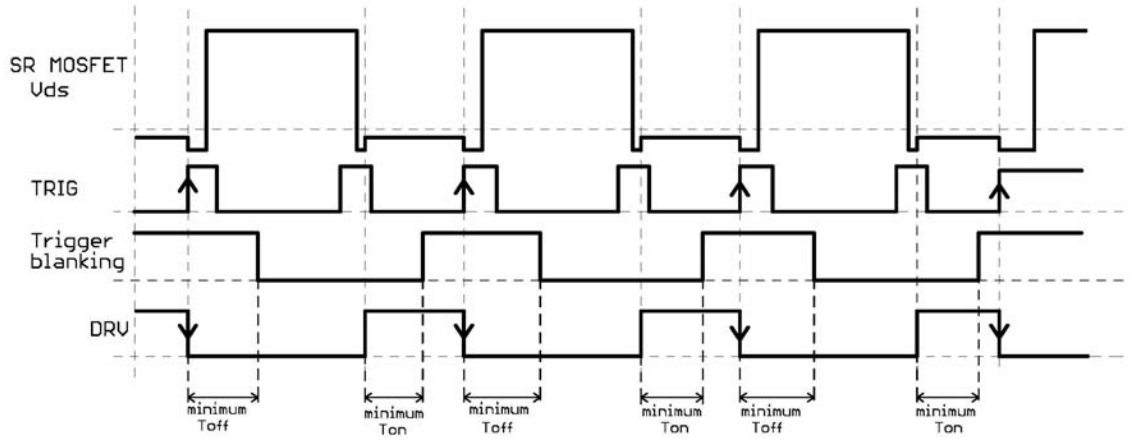


Figure 41. Trigger Input Functionality Waveforms

The NCP4303 operation can be disabled using the trigger/disable input. If the trigger/disable input is pulled up (above 1.5 V) the driver is disabled immediately. In some cases, the driver is activated one more time by the current sense because the trigger signal is still blanked. This final drive pulse lasts only for the minimum on time period. If the trigger signal is high for more than 100 μs, the driver enters standby mode. Note that a short pulse (2 μs maximally) can appear on the DRV pin during transition to sleep mode in case there was no switching on the CS input prior transition − refer to Figure 44. This behavior is related to the internal IC logic structure and may cause unwanted SR MOSFET activation in some applications. It is recommended to disable NCP4303 driver via V_{CC} pin in such cases − refer to Figure 61. The IC consumption is reduced to 390 μA during the standby mode. When trigger input voltage is decreased again the device recovers operation in 500 ns. If the IC is enabled in the time the current sense input voltage is negative (secondary current flows through the Shottky or body diode) the IC waits for another switching cycle to turn−on the SR MOSFET – refer to Figures 42, 43 44, and 45.

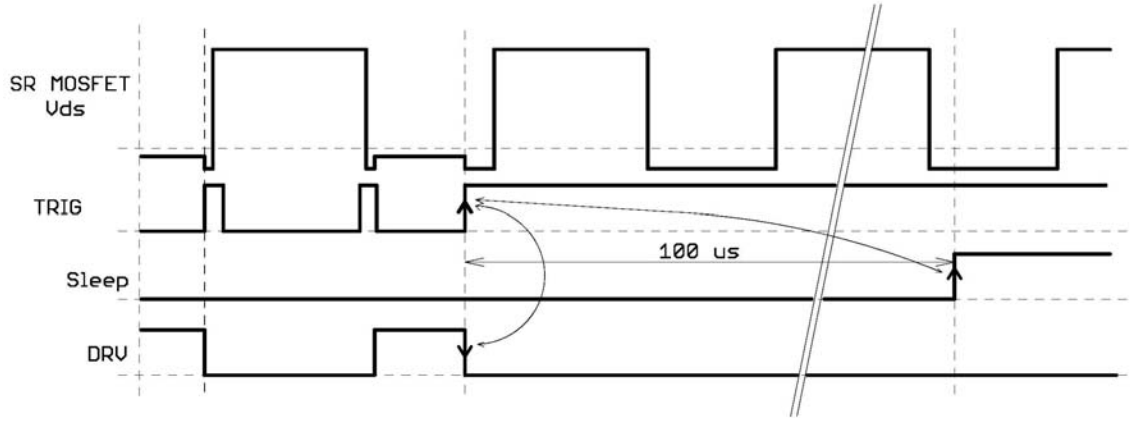


Figure 42. Operating Waveforms for the Trig/Disable Input – Device Sleep Mode Transition – Case 1

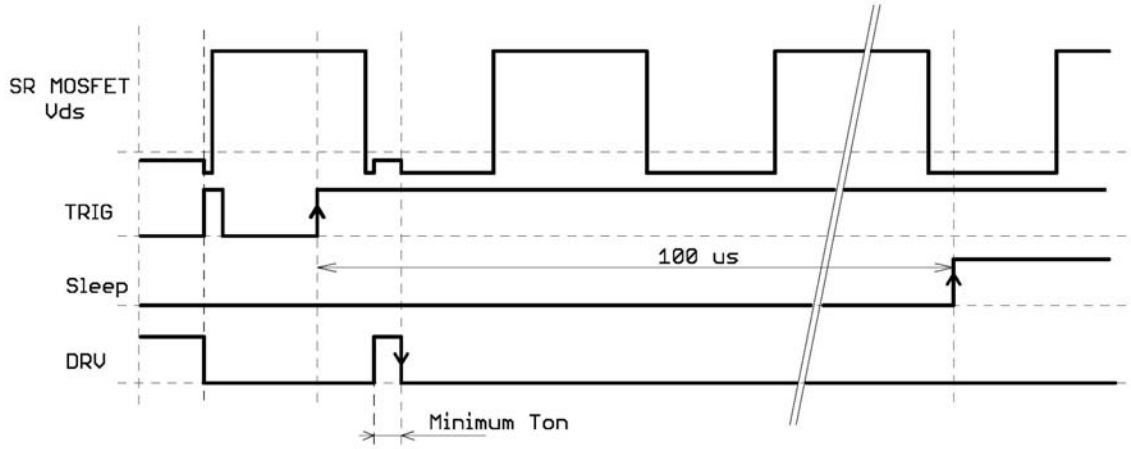


Figure 43. Operating Waveforms for the Trig/Disable Input – Device Sleep Mode Transition – Case 2

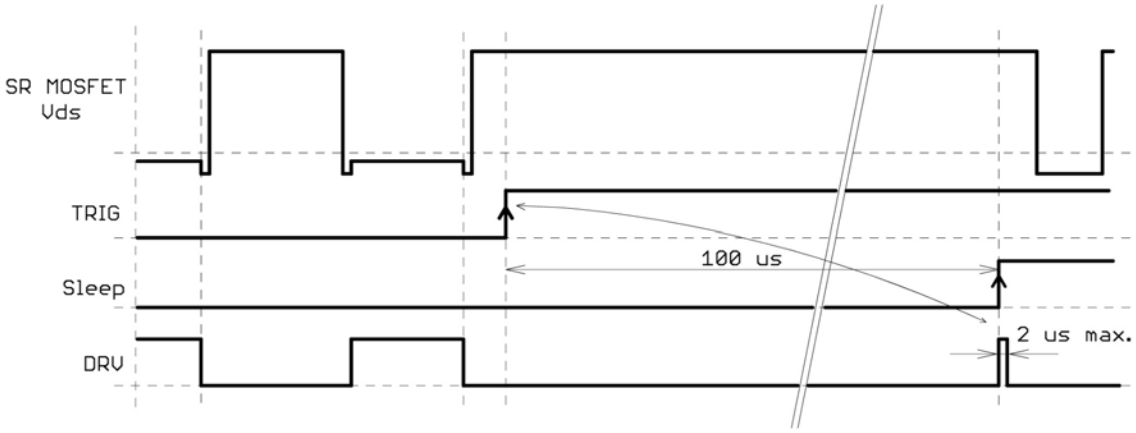


Figure 44. Operating Waveforms for the Trig/Disable Input − Device Sleep Mode Transition − Case 3

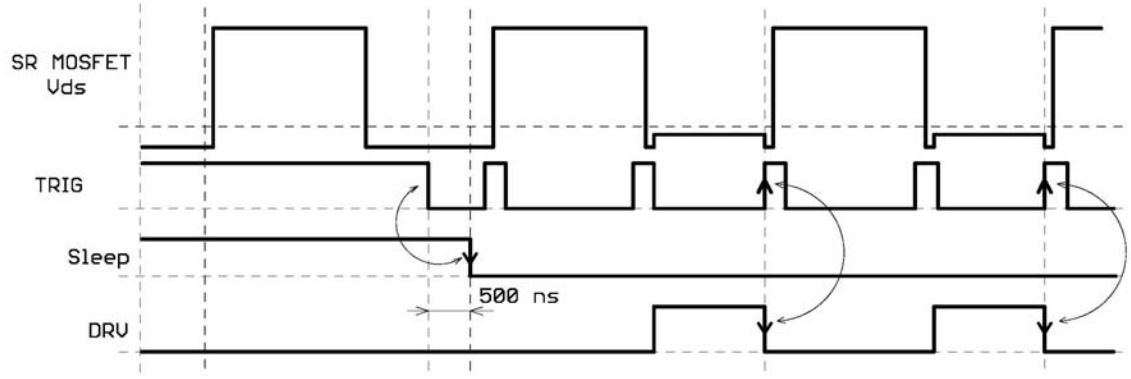


Figure 45. Operating Waveforms for the Trig/Disable Input –Wake−up from Sleep Mode

If the trigger signal comes periodically and the trigger pulse overlaps the SR MOSFET drain positive voltage (i.e. overlaps the whole SR MOSFET body diode off time period), the driver is disabled for the next cycle – refer to Figure 46.

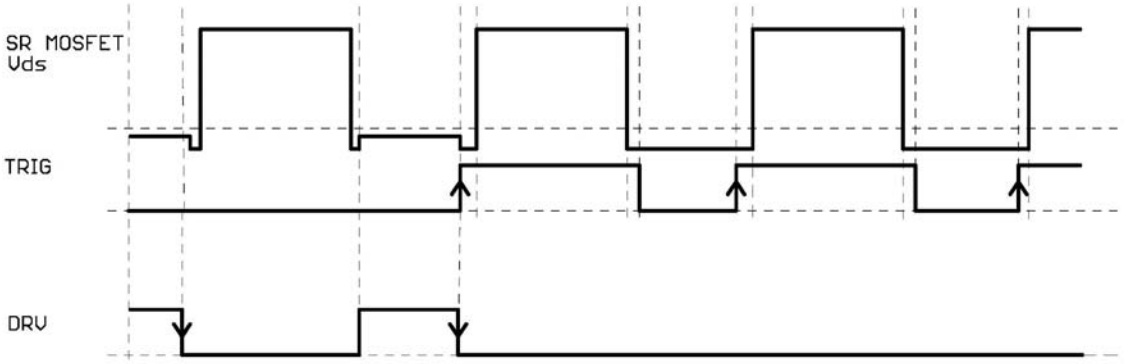


Figure 46. Operating Waveforms for the Trig/Disable Input with a Trigger Signal that is Periodical and Overlaps CS (SR MOSFET Vds) High Level

Note that the trigger input is an ultrafast input that doesn't feature any internal filtering and reacts even on very narrow voltage pulses. Thus it is wise to keep this input on a low impedance path and provide it with a clean triggering signal.

A typical application schematic of a flyback converter that is operated in deep CCM mode can be seen in Figure 47. In this application the trigger signal is taken directly from the flyback controller driver output and transmitted to the secondary side by pulse transformer TR2. Because the trigger input is rising edge sensitive, it is not necessary to transmit the entire primary driver pulse to the secondary. The coupling capacitor C5 is used to allow pulse transformer core reset and also to prepare a needle pulse (a pulse with width lower than 100 ns) to be transmitted to the NCP4303 trigger input. The advantage of needle trigger pulse usage is that the required volt−second product of the pulse transformer is very low and that allows the designer to use very small and cheap magnetics. The trigger transformer can be for instance prepared on a small toroidal ferrite core with diameter of 8 mm. Proper safety insulation between primary and secondary sides can be easily assured by using triple insulated wire for one or even both windings.

The primary MOSFET gate voltage rising edge is delayed by external circuitry consisting of transistors Q1, Q2 and surrounding components. The primary MOSFET is thus turned−on with a slight delay so that the secondary controller turns−off the SR MOSFET by trigger signal prior to the primary switching. This method reduces the commutation losses and the SR MOSFET drain voltage spike, which results in improved efficiency.

It is also possible to use capacitive coupling (use additional capacitor with safety insulation) between the primary and secondary to transmit the trigger signal. We do not recommend this technique as the parasitic capacitive currents between primary and secondary may affect the trigger signal and thus overall system functionality.

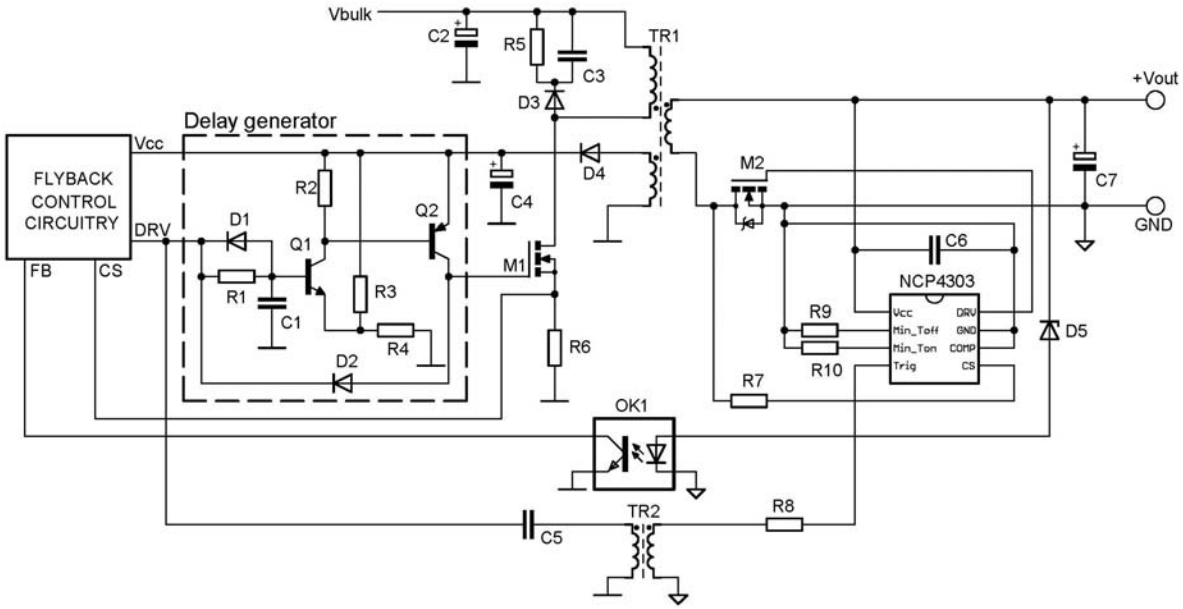


Figure 47. Optional Application Schematic When NCP4303 is Used in CCM Flyback Converter and Trigger Input is Implemented to Maximize Efficiency

Minimum T_{on} and T_{off} Adjustment

The NCP4303 offers adjustable minimum ON and OFF time periods that ease the implementation of the synchronous rectification system in a power supply. These timers avoid false triggering on the CS input after the MOSFET is turned on or off. The adjustment is based on an internal timing capacitance and external resistors connected to the GND pin – refer to Figure 48 for better understanding.

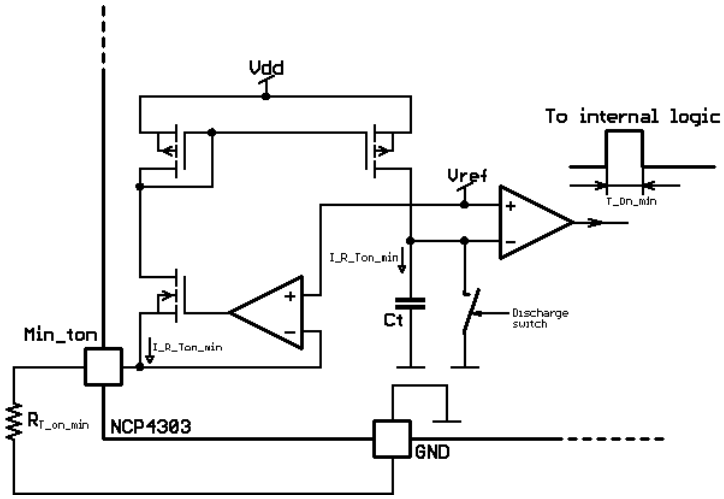


Figure 48. Internal Connection of the Min_Ton Generator (the Min_Toff Works in the Same Way)

Current through the Min_Ton adjust resistor can be calculated as:

$$I_{R_Ton_min} = \frac{V_{ref}}{R_{Ton_min}} \quad \text{(eq. 4)}$$

As the same current is used for the internal timing capacitor (Ct) charging, one can calculate the minimum on−time duration using this equation.

$$T_{on_min} = C_t \cdot \frac{V_{ref}}{I_{R_Ton_min}} = C_t = \frac{V_{ref}}{\frac{V_{ref}}{R_{Ton_min}}} \quad \text{(eq. 5)}$$

$$= C_t \cdot R_{Ton_min}$$

As can be seen from Equation 5, the minimum ON and OFF times are independent of the V_{ref} or V_{CC} level. The internal capacitor size would be too high if we would use directly $I_{R_Ton_min}$ current thus this current is decreased by the internal current mirror ratio. One can then calculate the minimum T_{on} and T_{off} blanking periods using below equations:

$$T_{on_min} = 9.82 * 10^{-11} * R_{T_on_min} + 4.66 * 10^{-8}\ [\mu s] \quad \text{(eq. 6)}$$

$$T_{off_min} = 9.56 * 10^{-11} * R_{T_off_min} + 5.397 * 10^{-8}\ [\mu s] \quad \text{(eq. 7)}$$

Note that the internal timing comparator delay affects the accuracy of Equations 6 and 7 when T_{on}/T_{off} times are selected near to their minimum possible values. Please refer to Figure 49 and 50 for measured minimum on and off time charts.

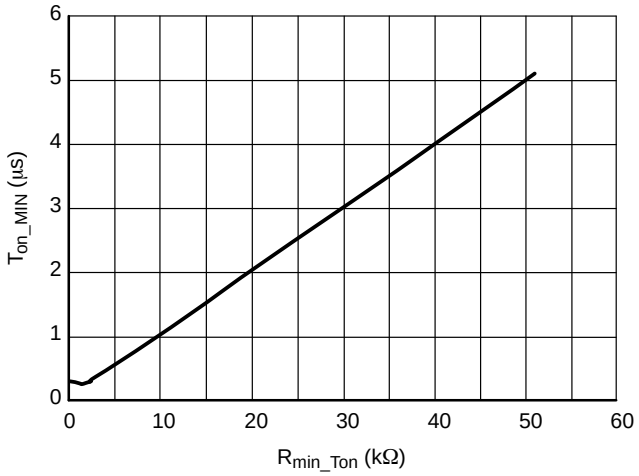


Figure 49. Min T_{on} Adjust Characteristic

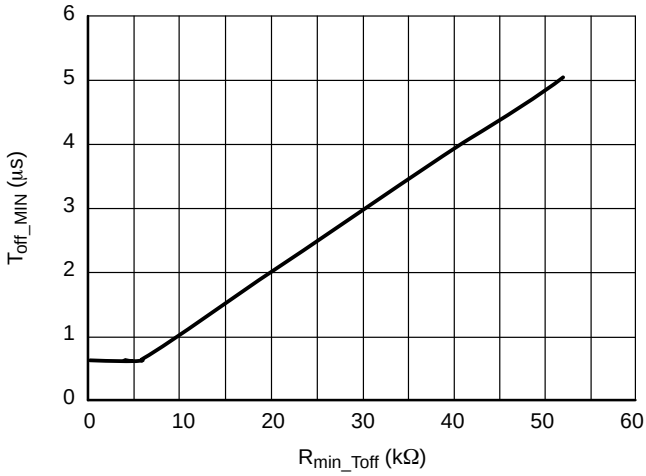


Figure 50. Min T_{off} Adjust Characteristic

The absolute minimum T_{on} duration is internally clamped to 300 ns and minimum T_{off} duration to 600 ns in order to prevent any potential issues with the minimum T_{on} and/or T_{off} input being shorted to GND.

Some applications may require adaptive minimum on and off time blanking periods. With NCP4303 it is possible to modulate blanking periods by using an external NPN transistor – refer to Figure 51. The modulation signal can be derived based on the load current or feedback regulator voltage.

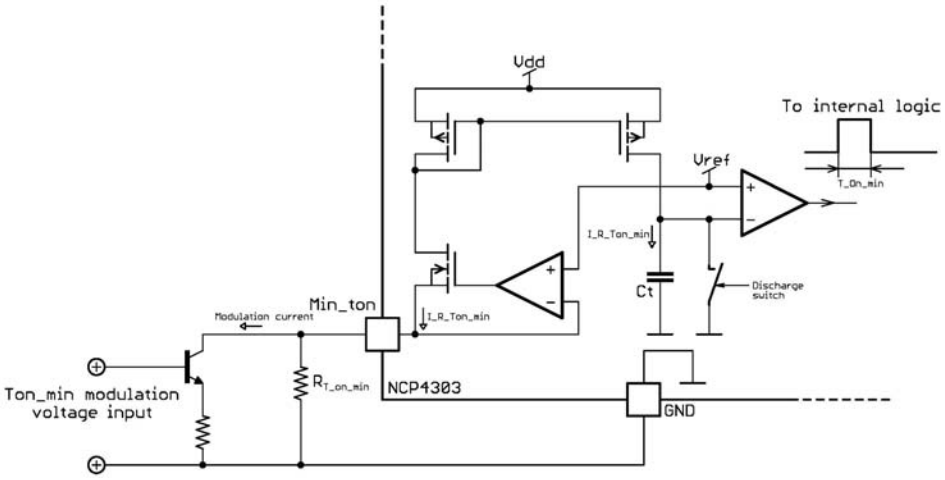


Figure 51. Possible Connection for Min T_{on} and T_{off} Modulation

In LLC applications with a very wide operating frequency range it is necessary to have very short minimum on time and off time periods in order to reach the required maximum operating frequency. However, when a LLC converter operates under low frequency, the minimum off time period may then be too short. To overcome possible issues with the LLC operating under low line and light load conditions, one can prolong the minimum off time blanking period by using resistors R_{drain1} and R_{drain2} connected from the opposite SR MOSFET drain – refer to Figure 52.

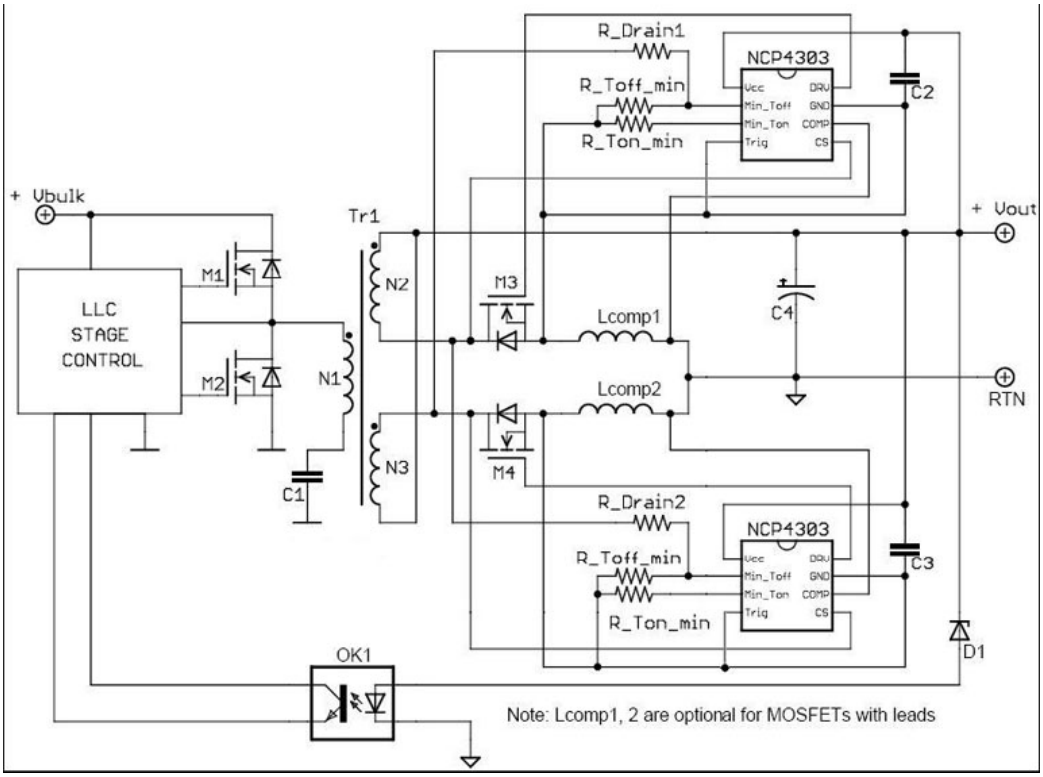


Figure 52. Possible Connection for Min Toff Prolongation in LLC Applications with Wide Operating Frequency Range

Note that R_{drain1} and R_{drain2} should be designed in such a way that the maximum pulse current into the Min_Toff adjust pin is below 10 mA. Voltage on the min T_{off} and T_{on} pins is clamped by internal zener protection to 10 V.

Power Dissipation Calculation

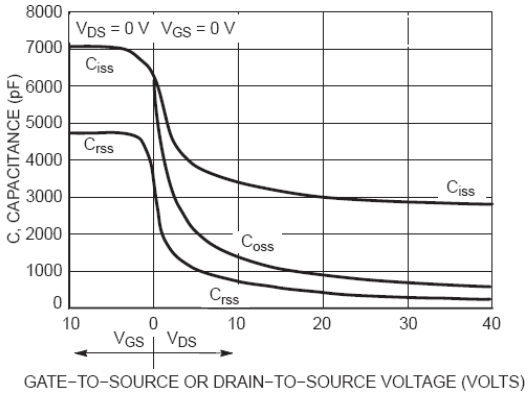
It is important to consider the power dissipation in the MOSFET driver of a SR system. If no external gate resistor is used and the internal gate resistance of the MOSFET is very low, nearly all energy losses related to gate charge are dissipated in the driver. Thus it is necessary to check the SR driver power losses in the target application to avoid over temperature and to optimize efficiency.

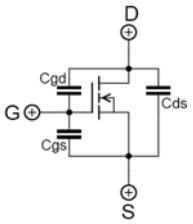
In SR systems the body diode of the SR MOSFET starts conducting before turn on because the $V_{th_cs_on}$ threshold level is below 0 V. On the other hand, the SR MOSFET turn off process always starts before the drain to source voltage rises up significantly. Therefore, the MOSFET switch always operates under Zero Voltage Switching (ZVS) conditions when implemented in a synchronous rectification system.

The following steps show how to approximately calculate the power dissipation and DIE temperature of the NCP4303A/B controller. Note that real results can vary due to the effects of the PCB layout on the thermal resistance.

Step 1 – MOSFET gate to source capacitance:

During ZVS operation the gate to drain capacitance does not have a Miller effect like in hard switching systems because the drain to source voltage is close to zero and its change is negligible.





$$C_{iss} = C_{gs} + C_{gd}$$
$$C_{rss} = C_{gd}$$
$$C_{oss} = C_{ds} + C_{gd}$$

Figure 53. Typical MOSFET Capacitances Dependency on V_{ds} and V_{gs} Voltages

Therefore, the input capacitance of a MOSFET operating in ZVS mode is given by the parallel combination of the gate to source and gate to drain capacitances (i.e. C_{iss} capacitance for given gate to source voltage). The total gate charge, Q_{g_total}, of most MOSFETs on the market is defined for hard switching conditions. In order to accurately calculate the driving losses in a SR system, it is necessary to determine the gate charge of the MOSFET for operation specifically in a ZVS system. Some manufacturers define this parameter as Q_{g_ZVS}. Unfortunately, most datasheets do not provide this data. If the C_{iss} (or Q_{g_ZVS}) parameter is not available then it will need to be measured. Please note that the input capacitance is not linear (as shown Figure 53) and it needs to be characterized for a given gate voltage clamp level.

Step 2 – Gate drive losses calculation:

Gate drive losses are affected by the gate driver clamp voltage. Gate driver clamp voltage selection depends on the type of MOSFET used (threshold voltage versus channel resistance). The total power losses (driving loses and conduction losses) should be considered when selecting the gate driver clamp voltage. Most of today's MOSFETs for SR systems feature low $R_{DS(on)}$ for 5 V V_{gs} voltage and thus it is beneficial to use NCP4303B. However, there is still a big group of MOSFETs on the market that require higher gate to source voltage − in this case the NCP4303A should be used.

The total driving loss can be calculated using the selected gate driver clamp voltage and the input capacitance of the MOSFET:

$$P_{DRV_total} = V_{CC} \cdot V_{clamp} \cdot C_{g_ZVS} \cdot f_{SW} \qquad \text{(eq. 8)}$$

Where:
V_{cc} is the NCP4303x supply voltage
V_{clamp} is the driver clamp voltage
C_{g_ZVS} is the gate to source capacitance of the MOSFET in ZVS mode
f_{sw} is the switching frequency of the target application

The total driving power loss won't only be dissipated in the IC, but also in external resistances like the external gate resistor (if used) and the MOSFET internal gate resistance (Figure 54). Because NCP4303A/B features a clamped driver, it's high side portion can be modeled as a regular driver switch with equivalent resistance and a series voltage source. The low side driver switch resistance does not drop

immediately at turn−off, thus it is necessary to use an equivalent value ($R_{drv_low_eq}$) for calculations. This method simplifies power losses calculations and still provides acceptable accuracy. Internal driver power dissipation can then be calculated using Equation 9:

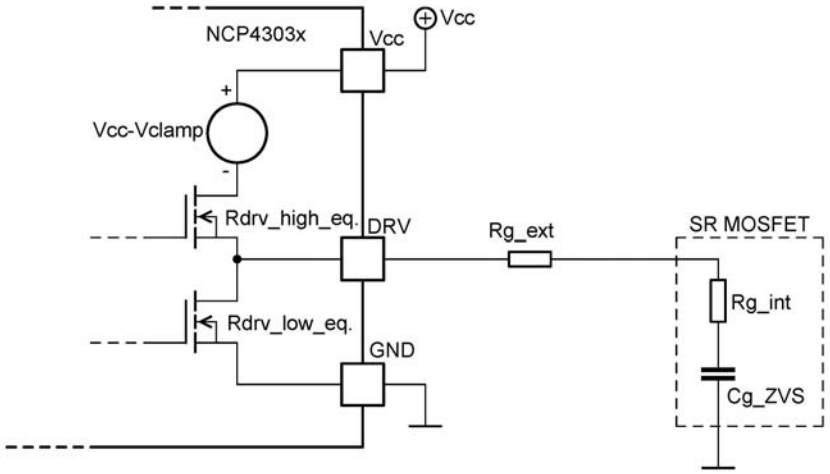


Figure 54. Equivalent Schematic of Gate Drive Circuitry

$$P_{DRV_IC} = \frac{1}{2} \cdot C_{g_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv_low_eq}}{R_{drv_low_eq} + R_{g_ext} + R_{g_int}} \right) + C_{g_ZVS} \cdot V_{clamp} \cdot f_{SW} \cdot \left(V_{CC} - V_{clamp} \right) \quad \text{(eq. 9)}$$

$$+ \frac{1}{2} \cdot C_{g_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv_high_eq}}{R_{drv_high_eq} + R_{g_ext} + R_{g_int}} \right)$$

Where:

$R_{drv_low_eq}$ is the NCP4303x driver low side switch equivalent resistance (1.55 Ω)

$R_{drv_high_eq}$ is the NCP4303x driver high side switch equivalent resistance (7 Ω)

R_{g_ext} is the external gate resistor (if used)

R_{g_int} is the internal gate resistance of the MOSFET

Step 3 – IC Consumption Calculation:

In this step, power dissipation related to the internal IC consumption is calculated. This power loss is given by the I_{CC} current and the IC supply voltage. The I_{CC} current depends on switching frequency and also on the selected min T_{on} and T_{off} periods because there is current flowing out from the min T_{on} and T_{off} pins. The most accurate method for calculating these losses is to measure the I_{cc} current when C_{load} = 0 nF and the IC is switching at the target frequency with given Min_Ton and Min_Toff adjust resistors. Refer also to Figure 55 for typical IC consumption charts when the driver is not loaded. IC consumption losses can be calculated as:

$$P_{ICC} = V_{CC} \cdot I_{CC} \quad \text{(eq. 10)}$$

Step 4 – IC DIE Temperature Arise Calculation:

The DIE temperature can be calculated now that the total internal power losses have been determined (driver losses plus internal IC consumption losses). The SO−8 package thermal resistance is specified in the maximum ratings table for a 35 μm thin copper layer with no extra copper plates on any pin (i.e. just 0.5 mm trace to each pin with standard soldering points are used).

The DIE temperature is calculated as:

$$T_{DIE} = \left(P_{DRV_IC} + P_{ICC} \right) \cdot R_{\theta J-A} + T_A \quad \text{(eq. 11)}$$

Where:

P_{DRV_IC} is the IC driver internal power dissipation

P_{Icc} is the IC control internal power dissipation

$R_{\theta JA}$ is the thermal resistance from junction to ambient

T_A is the ambient temperature

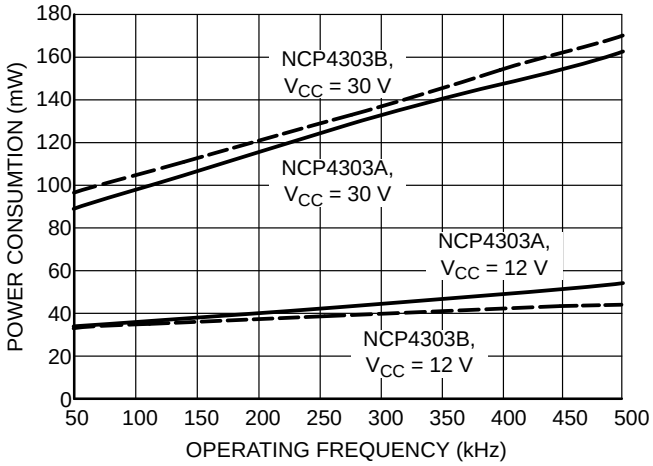


Figure 55. IC Power Consumption as a Function of Frequency for C_{load} = 0 nF, $R_{ton_min} = R_{toff_min}$ = 5 kΩ

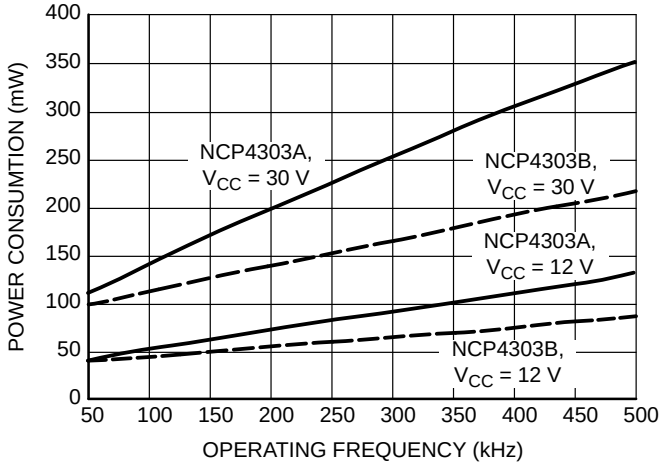


Figure 56. IC Power Consumption as a Function of Frequency for C_{load} = 1 nF, $R_{ton_min} = R_{toff_min}$ = 5 kΩ

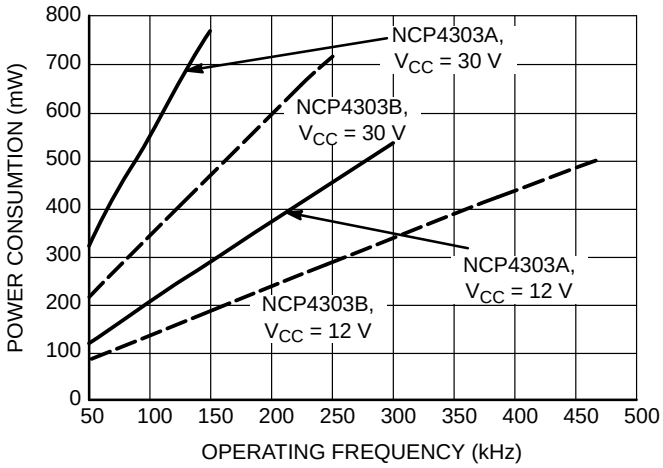


Figure 57. IC Power Consumption as a Function of Frequency for C_{load} = 10 nF, $R_{ton_min} = R_{toff_min}$ = 5 kΩ

65 W Adapter Design Example

This is wide range input application that uses NCP4303A. Application enters CCM mode for full load and Vin < 130 Vac. Efficiency results measured on this application can be seen in Figures 58 and 59. Application schematic of the 12 V/ 5.5 A adapter can be seen in Figure 60.

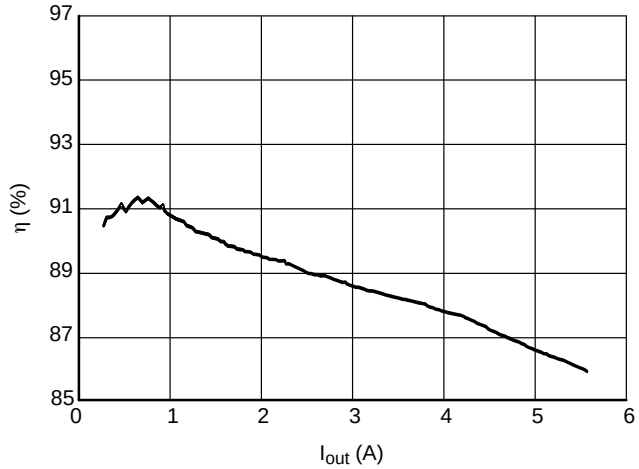


Figure 58.

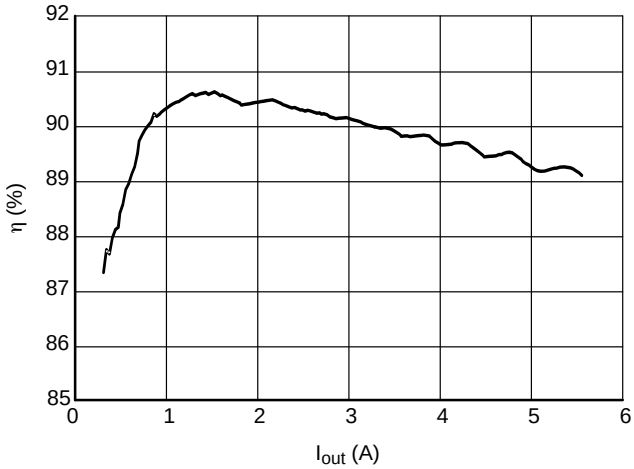


Figure 59.

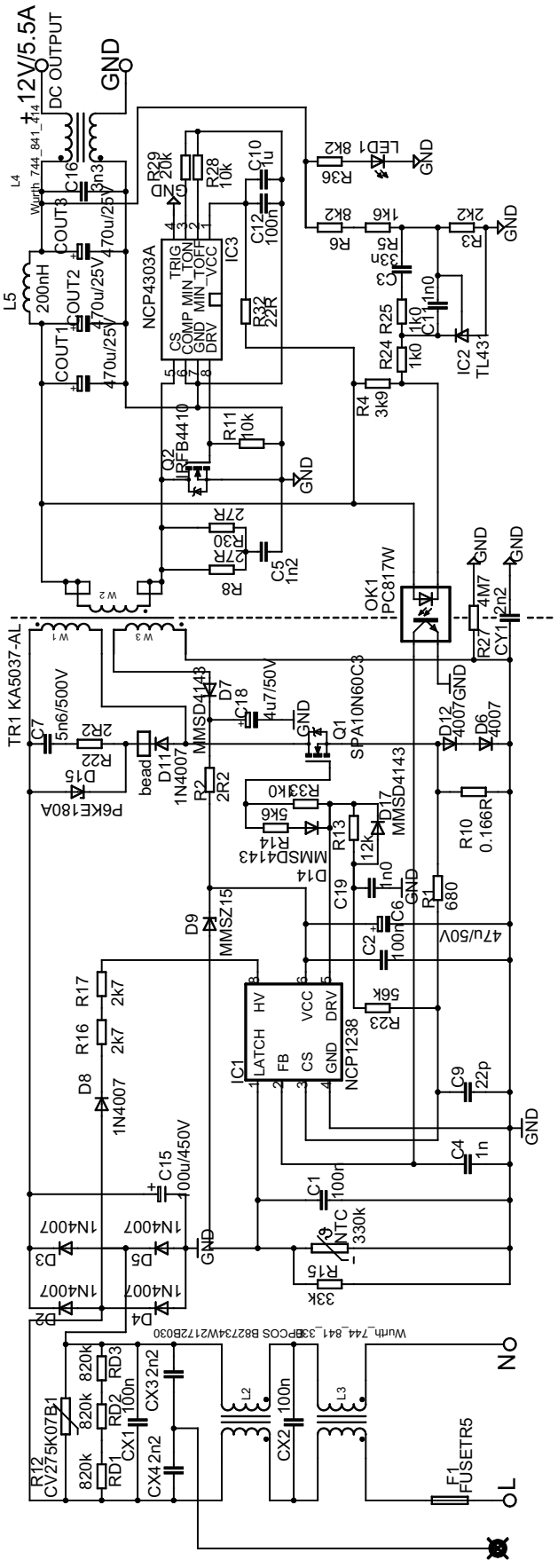


Figure 60. 65 W Adapter, V_{in} = 85 − 265 Vac, V_{out} = 12 V / 5.5 A

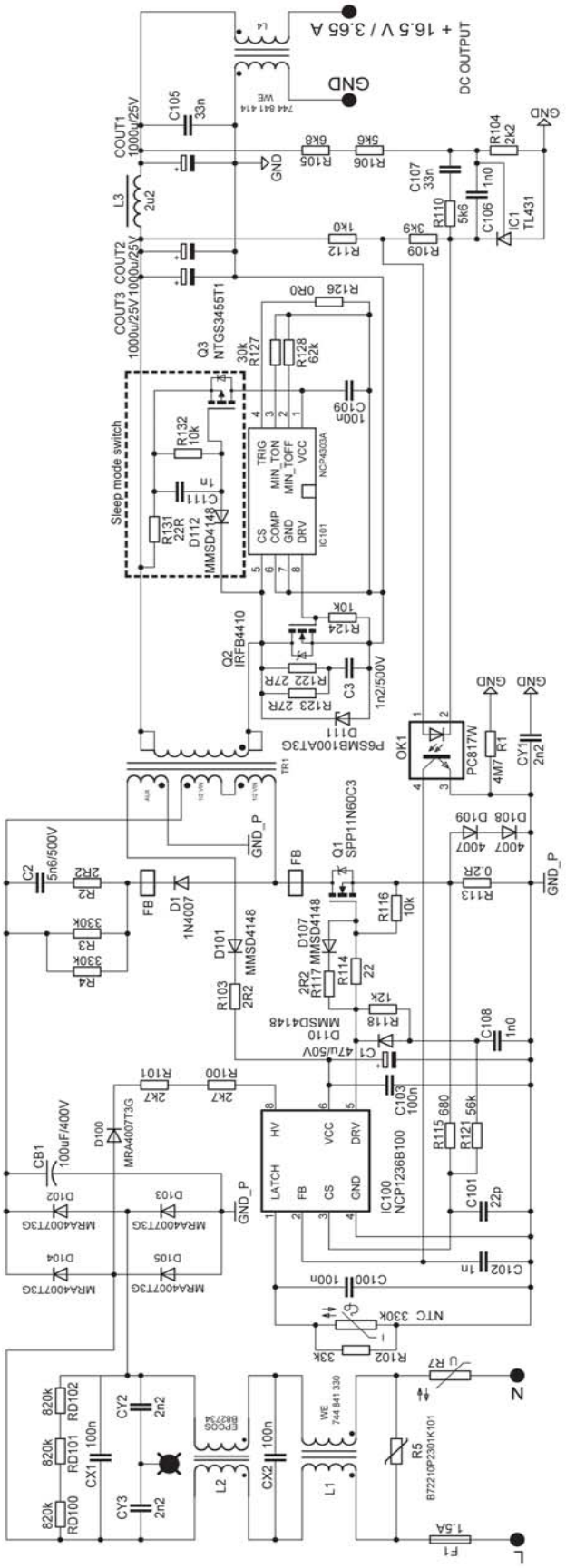


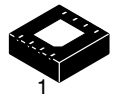
Figure 61. CCM Flyback Application with SR Sleep Mode Implemented via VCC Pin

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

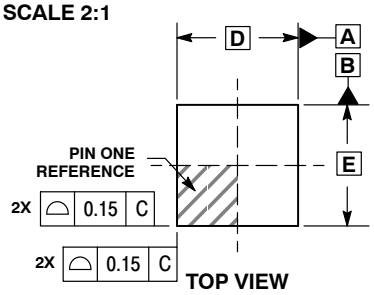
ON Semiconductor®

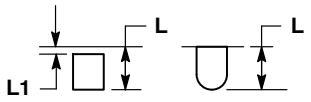
DFN8, 4x4
CASE 488AF−01
ISSUE C

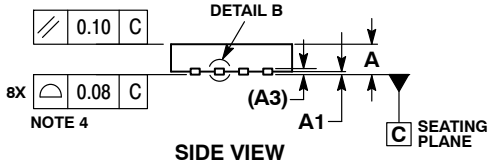
DATE 15 JAN 2009

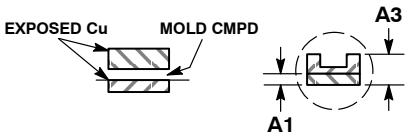


SCALE 2:1



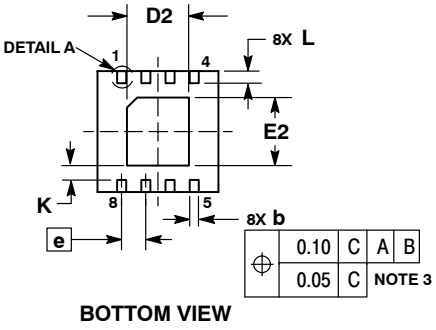




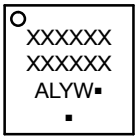


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

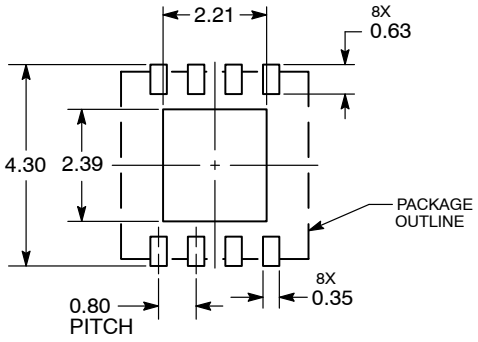


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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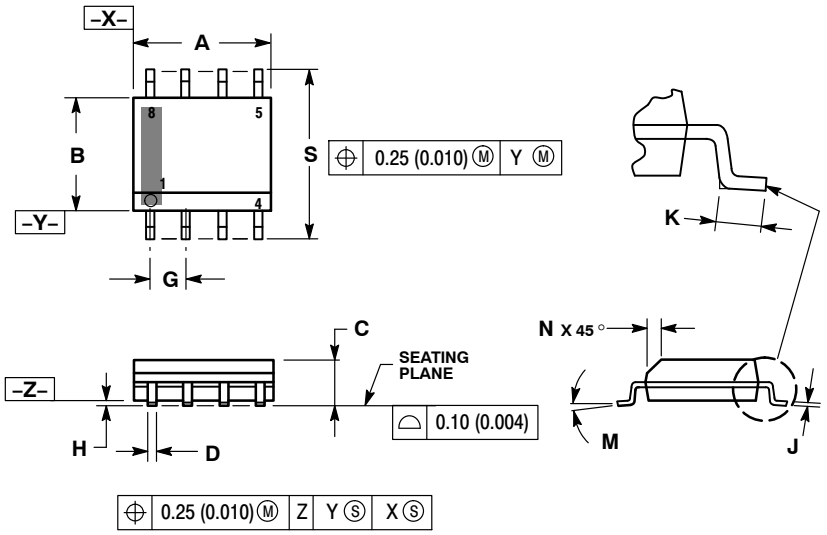
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

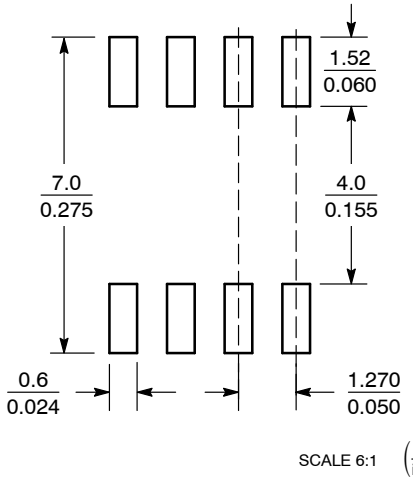
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

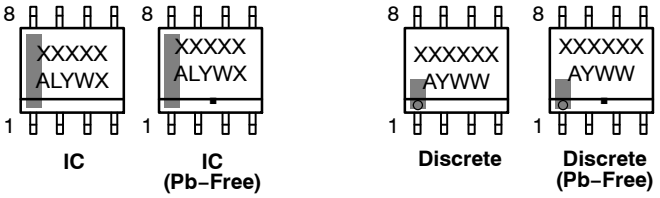
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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