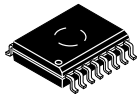


MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

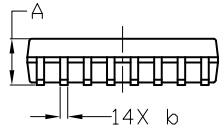
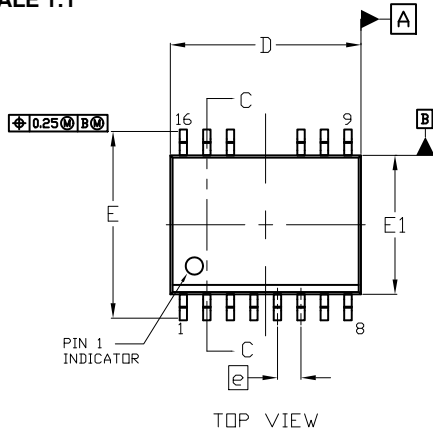
ON Semiconductor®



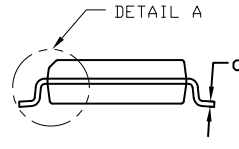
1
SCALE 1:1

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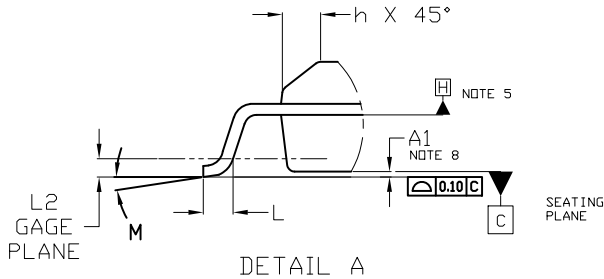
DATE 17 FEB 2021



SIDE VIEW



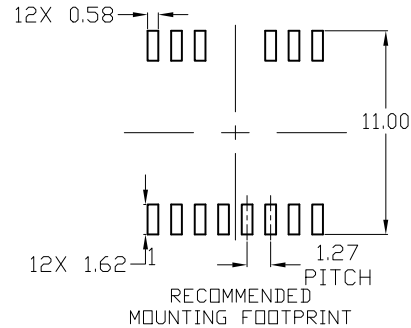
SECTION C-C



DETAIL A

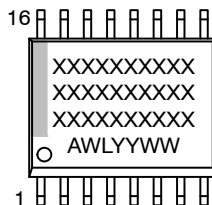
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
 4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE.
 5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
 7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
 8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.35	2.50	2.65
A1	0.10	0.18	0.25
b	0.35	0.42	0.49
c	0.25 REF		
D	10.15	10.30	10.45
E	10.05	10.30	10.55
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25	---	0.75
L	0.50	---	0.90
L2	0.25 REF		
M	0°	---	7°



■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRM/D](#).

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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