

# MC100LVEL29

## 3.3 V ECL Dual Differential Data and Clock D Flip-Flop with Set and Reset

### Description

The MC100LVEL29 is a dual master-slave flip-flop. The device features fully differential Data and Clock inputs as well as outputs. The MC100LVEL29 is pin and functionally equivalent to the MC100EL29. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to  $V_{EE}$  and the  $\bar{D}$  input will bias around  $V_{CC}/2$ . The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

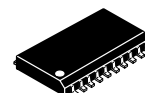
### Features

- 1100 MHz Flip-Flop Toggle Frequency
- ESD Protection: > 2 kV Human Body Model
- 580 ps Typical Propagation Delays
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)  
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 313 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



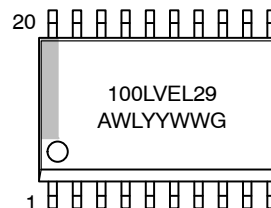
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SOIC-20 WB  
DW SUFFIX  
CASE 751D-05

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device           | Package                 | Shipping†        |
|------------------|-------------------------|------------------|
| MC100LVEL29DWG   | SOIC-20 WB<br>(Pb-Free) | 38 Units / Tube  |
| MC100LVEL29DWR2G | SOIC-20 WB<br>(Pb-Free) | 1000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LEVEL29

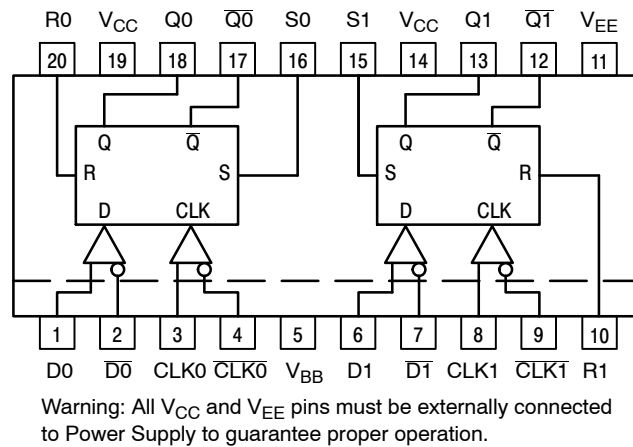


Figure 1. Logic Diagram and Pinout: 20-Lead SOIC (Top View)

Table 1. PIN DESCRIPTION

| PIN                                       | FUNCTION                      |
|---|-------------------------------|
| D0, $\overline{D0}$ ; D1, $\overline{D1}$ | ECL Differential Data Inputs  |
| R0, R1                                    | ECL Reset Inputs              |
| CLK0, $\overline{CLK0}$                   | ECL Differential Clock Inputs |
| CLK1, $\overline{CLK1}$                   | ECL Differential Clock Inputs |
| S0, S1                                    | ECL Set Inputs                |
| Q0, $\overline{Q0}$ ; Q1, $\overline{Q1}$ | ECL Differential Data Outputs |
| $V_{BB}$                                  | Reference Voltage Output      |
| $V_{CC}$                                  | Positive Supply               |
| $V_{EE}$                                  | Negative Supply               |

Table 2. TRUTH TABLE

| R | S | D | CLK | Q     | $\overline{Q}$ |
|---|---|---|-----|-------|----------------|
| L | L | L | Z   | L     | H              |
| L | L | H | Z   | H     | L              |
| H | L | X | X   | L     | H              |
| L | H | X | X   | H     | L              |
| H | H | X | X   | Undef | Undef          |

Z = LOW to HIGH Transition  
X = Don't Care

Table 3. MAXIMUM RATINGS

| Symbol        | Parameter  | Condition 1                                    | Condition 2                            | Rating            | Unit                        |
|---------------|--|--|--|-------------------|-----------------------------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |  | 8 to 0            | V                           |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0\text{ V}$                          |  | -8 to 0           | V                           |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>-6 to 0 | V                           |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100         | mA                          |
| $I_{BB}$      | $V_{BB}$ Sink/Source                               |  |  | $\pm 0.5$         | mA                          |
| $T_A$         | Operating Temperature Range                        |  |  | -40 to +85        | $^{\circ}\text{C}$          |
| $T_{stg}$     | Storage Temperature Range                          |  |  | -65 to +150       | $^{\circ}\text{C}$          |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-20 WB<br>SOIC-20 WB               | 90<br>60          | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-20 WB                             | 30 to 35          | $^{\circ}\text{C}/\text{W}$ |
| $T_{sol}$     | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260 $^{\circ}\text{C}$          |  | 265               | $^{\circ}\text{C}$          |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC100LEVEL29

**Table 4. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

| Symbol      | Characteristic  | -40°C       |      |      | 25°C        |      |      | 85°C        |      |      | Unit          |
|-------------|---|-------------|------|------|-------------|------|------|-------------|------|------|---------------|
|             |   | Min         | Typ  | Max  | Min         | Typ  | Max  | Min         | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current  |             | 35   | 50   |             | 35   | 50   |             | 35   | 50   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)  | 2215        | 2295 | 2420 | 2275        | 2345 | 2420 | 2275        | 2345 | 2420 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)   | 1470        | 1605 | 1745 | 1490        | 1595 | 1680 | 1490        | 1595 | 1680 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2135        |      | 2420 | 2135        |      | 2420 | 2135        |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1490        |      | 1825 | 1490        |      | 1825 | 1490        |      | 1825 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1.92        |      | 2.04 | 1.92        |      | 2.04 | 1.92        |      | 2.04 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{pp} < 500\text{ mV}$<br>$V_{pp} \geq 500\text{ mV}$ |             |      |      |             |      |      |             |      |      | V             |
|             |   | 1.3         |      | 2.9  | 1.2         |      | 2.9  | 1.2         |      | 2.9  |               |
|             |   | 1.5         |      | 2.9  | 1.4         |      | 2.9  | 1.4         |      | 2.9  |               |
| $I_{IH}$    | Input HIGH Current  |             |      | 150  |             |      | 150  |             |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>$D_n$<br>$\overline{D}_n$  | 0.5<br>-300 |      |      | 0.5<br>-300 |      |      | 0.5<br>-300 |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol      | Characteristic  | -40°C       |       |       | 25°C        |       |       | 85°C        |       |       | Unit          |
|-------------|---|-------------|-------|-------|-------------|-------|-------|-------------|-------|-------|---------------|
|             |   | Min         | Typ   | Max   | Min         | Typ   | Max   | Min         | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current  |             | 35    | 50    |             | 35    | 50    |             | 35    | 50    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)  | -1085       | -1005 | -880  | -1025       | -955  | -880  | -1025       | -955  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)   | -1830       | -1695 | -1555 | -1810       | -1705 | -1620 | -1810       | -1705 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1165       |       | -880  | -1165       |       | -880  | -1165       |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1810       |       | -1475 | -1810       |       | -1475 | -1810       |       | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1.38       |       | -1.26 | -1.38       |       | -1.26 | -1.38       |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{pp} < 500\text{ mV}$<br>$V_{pp} \geq 500\text{ mV}$ |             |       |       |             |       |       |             |       |       | V             |
|             |   | -2.0        |       | -0.4  | -2.1        |       | -0.4  | -2.1        |       | -0.4  |               |
|             |   | -1.8        |       | -0.4  | -1.9        |       | -0.4  | -1.9        |       | -0.4  |               |
| $I_{IH}$    | Input HIGH Current  |             |       | 150   |             |       | 150   |             |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>$D_n$<br>$\overline{D}_n$  | 0.5<br>-300 |       |       | 0.5<br>-300 |       |       | 0.5<br>-300 |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

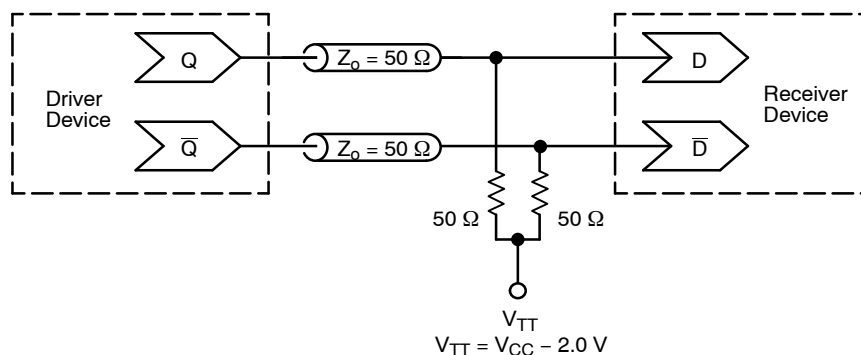
# MC100LVEL29

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol                 | Characteristic                             | -40°C      |     |            | 25°C       |            |            | 85°C       |     |            | Unit |
|------------------------|--|------------|-----|------------|------------|------------|------------|------------|-----|------------|------|
|                        |  | Min        | Typ | Max        | Min        | Typ        | Max        | Min        | Typ | Max        |      |
| $f_{\max}$             | Maximum Toggle Frequency                   | 1.1        |     |            | 1.1        |            |            | 1.1        |     |            | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>CLK<br>S, R | 480<br>480 |     | 680<br>700 | 500<br>500 | 580<br>720 | 700<br>720 | 520<br>520 |     | 720<br>740 | ps   |
| $t_S$<br>$t_H$         | Setup Time<br>Hold Time                    | 0<br>100   |     |            | 0<br>100   |            |            | 0<br>100   |     |            | ps   |
| $t_{RR}$               | Set/Reset Recovery                         | 100        |     |            | 100        |            |            | 100        |     |            | ps   |
| $t_{PW}$               | Minimum Pulse Width<br>CLK, Set, Reset     | 400        |     |            | 400        |            |            | 400        |     |            | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter                      |            | TBD |            |            | TBD        |            |            | TBD |            | ps   |
| $V_{PP}$               | Input Swing (Note 2)                       | 150        |     | 1000       | 150        |            | 1000       | 150        |     | 1000       | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q (20%–80%)         | 280        |     | 550        | 280        |            | 550        | 280        |     | 550        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters guaranteed.



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| b   | 0.35        | 0.49  |
| c   | 0.23        | 0.32  |
| D   | 12.65       | 12.95 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| θ   | 0°          | 7°    |

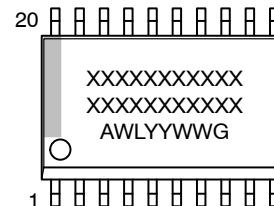
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |             |  |
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