

# MC1489, MC1489A

## Quad Line EIA-232D Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

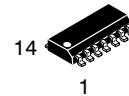
### Features

- Input Resistance – 3.0 k to 7.0 k $\Omega$
- Input Signal Range –  $\pm 30$  V
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering
- Pb-Free Packages are Available

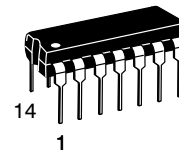


**ON Semiconductor**<sup>®</sup>

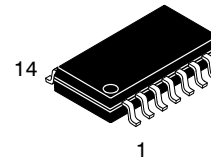
<http://onsemi.com>



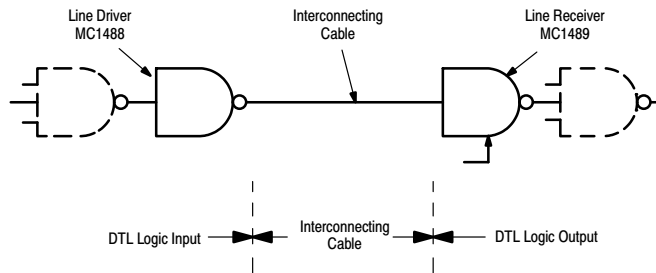
**SOIC-14  
D SUFFIX  
CASE 751A**



**PDIP-14  
P SUFFIX  
CASE 646**

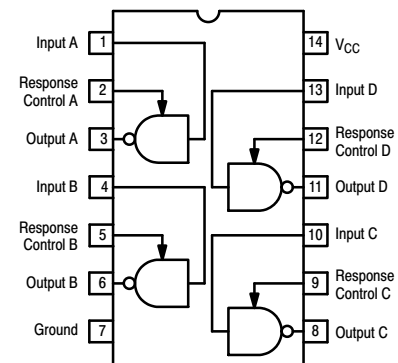


**SOEIAJ-14  
M SUFFIX  
CASE 965**



**Figure 1. Simplified Application**

### PIN CONNECTIONS



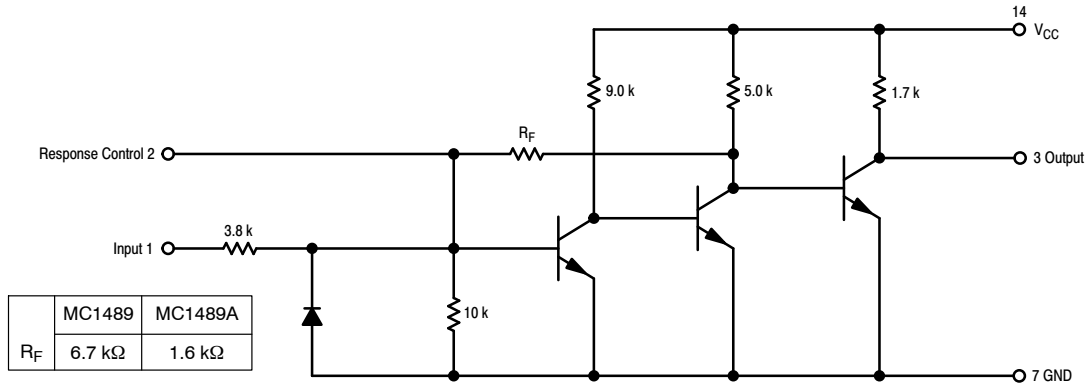
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

# MC1489, MC1489A



**Figure 2. Representative Schematic Diagram**  
(1/4 of Circuit Shown)

# MC1489, MC1489A

## MAXIMUM RATINGS (T<sub>A</sub> = + 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	10	Vdc
Input Voltage Range	V <sub>IR</sub>	± 30	Vdc
Output Load Current	I <sub>L</sub>	20	mA
Power Dissipation (Package Limitation, SOIC-14 and Plastic Dual In-Line Package) Derate above T <sub>A</sub> = + 25°C	P <sub>D</sub> 1/θ <sub>JA</sub>	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T <sub>A</sub>	0 to + 75	°C
Storage Temperature Range	T <sub>stg</sub>	- 65 to + 175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V<sub>CC</sub> = + 5.0 Vdc ± 10%, T<sub>A</sub> = 0 to + 75°C, unless otherwise noted)

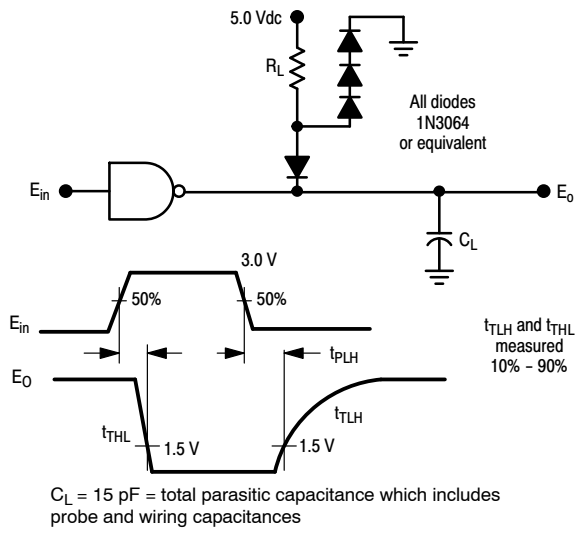
Characteristics	Symbol	Min	Typ	Max	Unit
Positive Input Current (V <sub>IH</sub> = + 25 Vdc) (V <sub>IH</sub> = + 3.0 Vdc)	I <sub>IH</sub>	3.6 0.43	- -	8.3 -	mA
Negative Input Current (V <sub>IH</sub> = - 25 Vdc) (V <sub>IH</sub> = - 3.0 Vdc)	I <sub>IL</sub>	- 3.6 - 0.43	- -	- 8.3 -	mA
Input Turn-On Threshold Voltage (T <sub>A</sub> = + 25°C, V <sub>OL</sub> ≤ 0.45 V)	V <sub>IH</sub>	1.0 1.75	- 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T <sub>A</sub> = + 25°C, V <sub>OH</sub> ≥ 2.5 V, I <sub>L</sub> = - 0.5 mA)	V <sub>IL</sub>	0.75 0.75	- 0.8	1.25 1.25	Vdc
Output Voltage High (V <sub>IH</sub> = 0.75 V, I <sub>L</sub> = - 0.5 mA) (Input Open Circuit, I <sub>L</sub> = - 0.5 mA)	V <sub>OH</sub>	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low (V <sub>IL</sub> = 3.0 V, I <sub>L</sub> = 10 mA)	V <sub>OL</sub>	-	0.2	0.45	Vdc
Output Short-Circuit Current	I <sub>OS</sub>	-	- 3.0	- 4.0	mA
Power Supply Current (All Gates "on," I <sub>out</sub> = 0 mA, V <sub>IH</sub> = + 5.0 Vdc)	I <sub>CC</sub>	-	16	26	mA
Power Consumption (V <sub>IH</sub> = + 5.0 Vdc)	P <sub>C</sub>	-	80	130	mW

## SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5.0 Vdc ± 1%, T<sub>A</sub> = + 25°C, See Figure 3.)

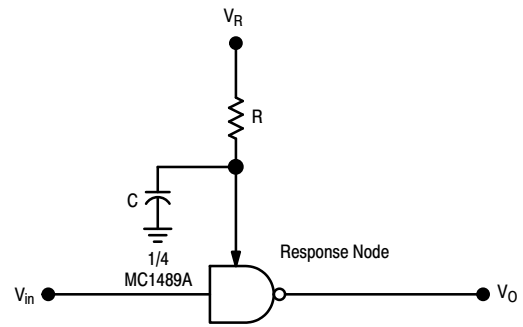
Propagation Delay Time (R <sub>L</sub> = 3.9 kΩ)	t <sub>PLH</sub>	-	25	85	ns
Rise Time (R <sub>L</sub> = 3.9 kΩ)	t <sub>TLH</sub>	-	120	175	ns
Propagation Delay Time (R <sub>L</sub> = 390 kΩ)	t <sub>PHL</sub>	-	25	50	ns
Fall Time (R <sub>L</sub> = 390 kΩ)	t <sub>THL</sub>	-	10	20	ns

# MC1489, MC1489A

## TEST CIRCUITS



**Figure 3. Switching Response**



**Figure 4. Response Control Node**

# MC1489, MC1489A

## TYPICAL CHARACTERISTICS

( $V_{CC} = 5.0 \text{ Vdc}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted)

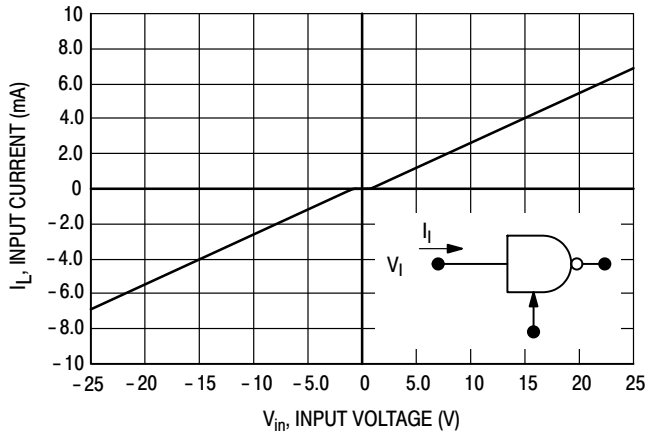


Figure 5. Input Current

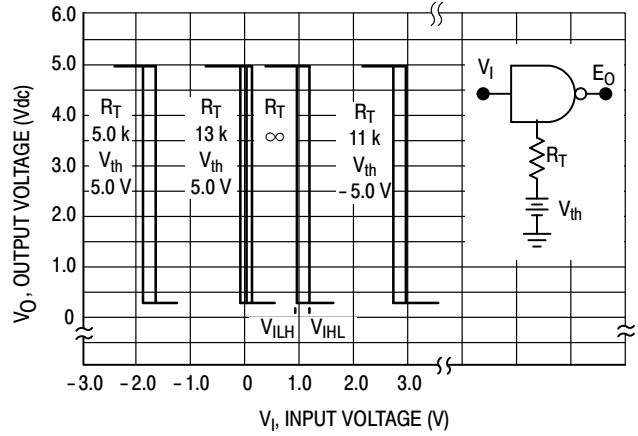


Figure 6. MC1489 Input Threshold Voltage Adjustment

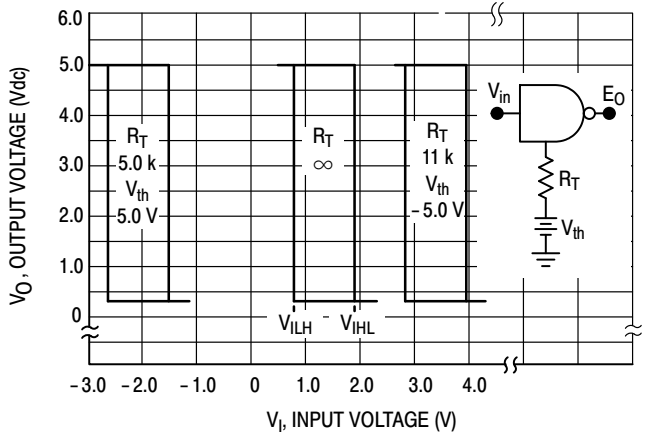


Figure 7. MC1489A Input Threshold Voltage Adjustment

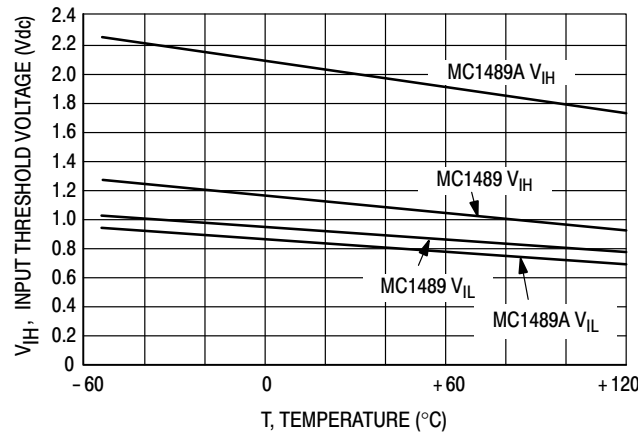


Figure 8. Input Threshold Voltage versus Temperature

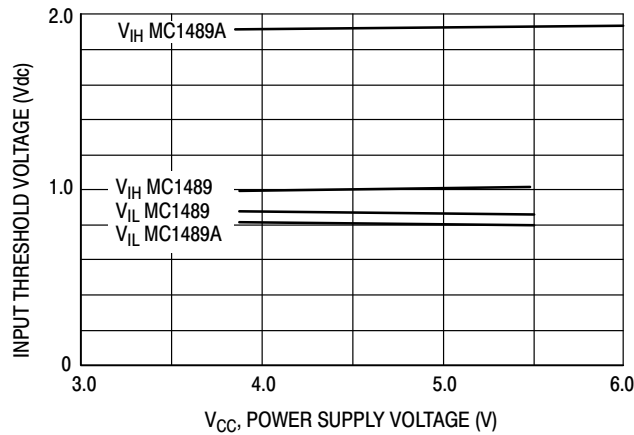


Figure 9. Input Threshold versus Power Supply Voltage

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one  $V_{BE}$ .

The receiver shall detect a voltage between - 3.0 and -25 V as a Logic "1" and inputs between 3.0 and 25 V as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical

turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 4, 6 and 7 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 10 and 11 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and DTL/TTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 12).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 13 where two receivers are slaved to the same line that must still meet the EIA-232D impedance requirement.

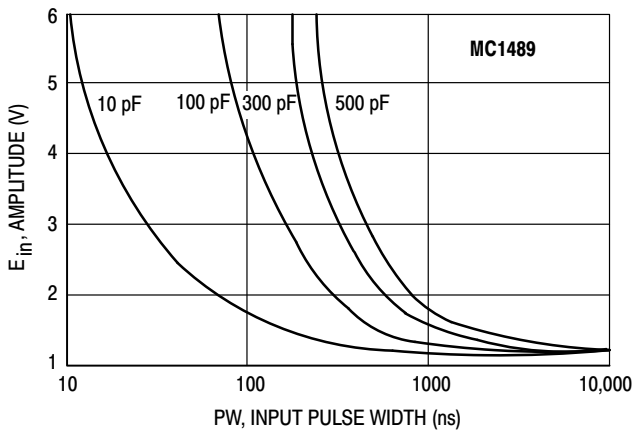


Figure 10. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

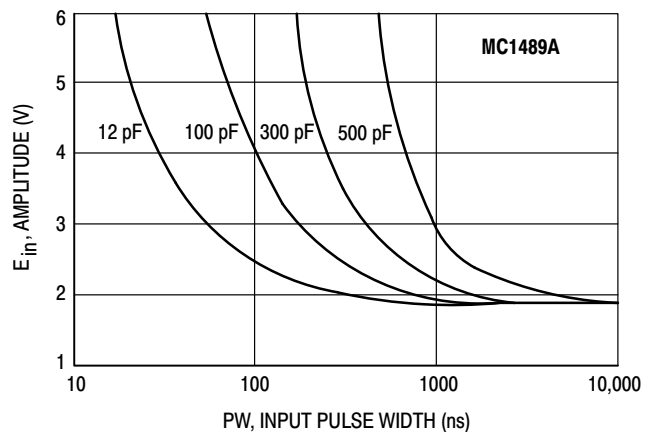


Figure 11. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

## MC1489, MC1489A

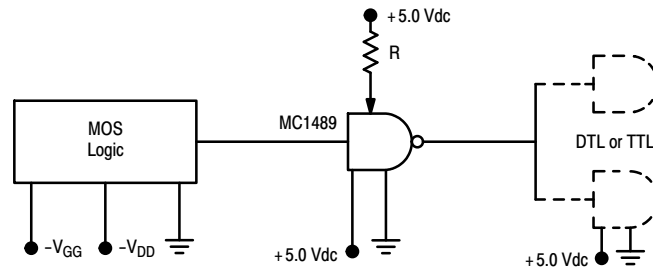


Figure 12. Typical Translator Application - MOS to DTL or TTL

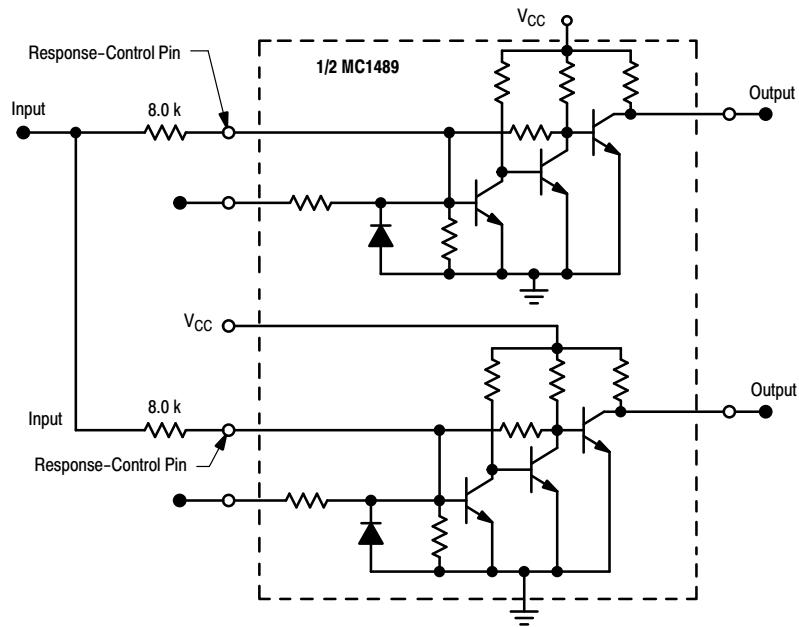


Figure 13. Typical Paralleling of Two MC1489, A Receivers to Meet EIA-232D

# MC1489, MC1489A

## ORDERING INFORMATION

Device	Package	Operating Temperature Range	Shipping <sup>†</sup>
MC1489D	SOIC-14	$T_A = 0 \text{ to } +75^\circ\text{C}$	55 Units/Rail
MC1489DG	SOIC-14 (Pb-Free)		
MC1489DR2	SOIC-14		2500 Tape & Reel
MC1489DR2G	SOIC-14 (Pb-Free)		
MC1489AD	SOIC-14		55 Units/Rail
MC1489ADG	SOIC-14 (Pb-Free)		
MC1489ADR2	SOIC-14		2500 Tape & Reel
MC1489ADR2G	SOIC-14 (Pb-Free)		
MC1489P	PDIP-14		25 Units/Rail
MC1489PG	PDIP-14 (Pb-Free)		
MC1489AP	PDIP-14		
MC1489APG	PDIP-14 (Pb-Free)		
MC1489M	SOEIAJ-14		50 Units/Rail
MC1489MG	SOEIAJ-14 (Pb-Free)		
MC1489MEL	SOEIAJ-14		2000 Tape & Reel
MC1489MELG	SOEIAJ-14 (Pb-Free)		
MC1489AM	SOEIAJ-14		50 Units/Rail
MC1489AMG	SOEIAJ-14 (Pb-Free)		
MC1489AMEL	SOEIAJ-14		2000 Tape & Reel
MC1489AMELG	SOEIAJ-14 (Pb-Free)		

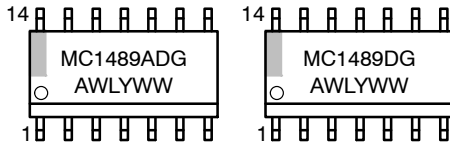
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



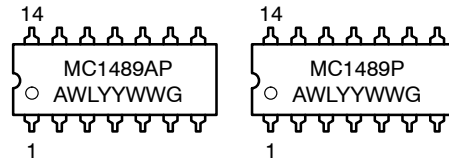
# MC1489, MC1489A

## MARKING DIAGRAMS

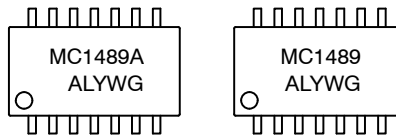
SOIC-14  
D SUFFIX  
CASE 751A



PDIP-14  
P SUFFIX  
CASE 646



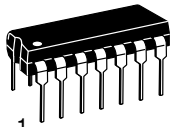
SOEIAJ-14  
M SUFFIX  
CASE 965



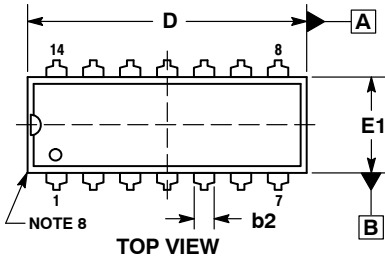
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

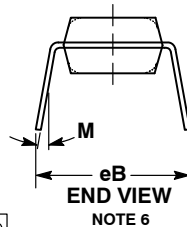
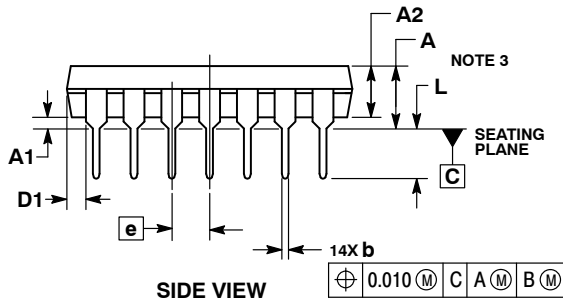
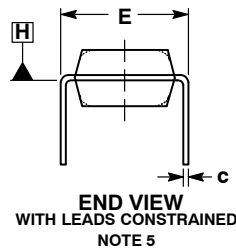


PDIP-14  
CASE 646-06  
ISSUE S

DATE 22 APR 2015

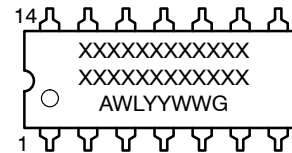
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

<b>DOCUMENT NUMBER:</b>	<b>98ASB42428B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PDIP-14</b>	<b>PAGE 1 OF 2</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**PDIP-14**  
**CASE 646-06**  
**ISSUE S**

DATE 22 APR 2015

STYLE 1:  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER  
 4. NO  
 CONNECTION  
 5. EMITTER  
 6. BASE  
 7. COLLECTOR  
 8. COLLECTOR  
 9. BASE  
 10. EMITTER  
 11. NO  
 CONNECTION  
 12. EMITTER  
 13. BASE  
 14. COLLECTOR

STYLE 2:  
 CANCELLED

STYLE 3:  
 CANCELLED

STYLE 4:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE  
 4. NO  
 CONNECTION  
 5. GATE  
 6. SOURCE  
 7. DRAIN  
 8. DRAIN  
 9. SOURCE  
 10. GATE  
 11. NO  
 CONNECTION  
 12. GATE  
 13. SOURCE  
 14. DRAIN

STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. NO CONNECTION  
 5. SOURCE  
 6. DRAIN  
 7. GATE  
 8. GATE  
 9. DRAIN  
 10. SOURCE  
 11. NO CONNECTION  
 12. SOURCE  
 13. DRAIN  
 14. GATE

STYLE 6:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 7:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON  
 CATHODE

STYLE 8:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE


STYLE 9:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

STYLE 10:  
 PIN 1. COMMON  
 CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON  
 CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 11:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 12:  
 PIN 1. COMMON CATHODE  
 2. COMMON ANODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. COMMON ANODE  
 7. COMMON CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

<b>DOCUMENT NUMBER:</b>	<b>98ASB42428B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PDIP-14</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

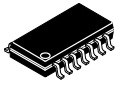
STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

<b>DOCUMENT NUMBER:</b>	<b>98ASB42565B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

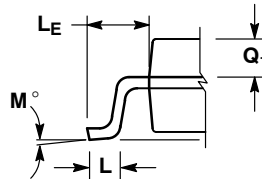
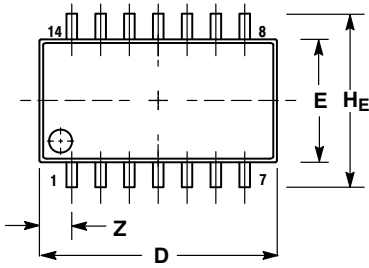
ON Semiconductor®



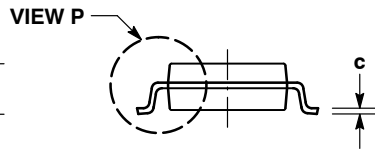
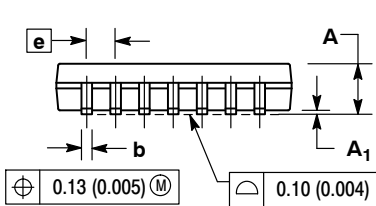
SCALE 1:1

SOEIAJ-14  
CASE 965-01  
ISSUE B

DATE 29 FEB 2008



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

<b>DOCUMENT NUMBER:</b>	<b>98ASH70108A</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>14 LD SOEIAJ</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

