3.3 V Serial Input MultiProtocol PLL Clock Synthesizer, Differential LVPECL Output

NB4N441

QFN−24
MN SUFFIX
CASE 485L

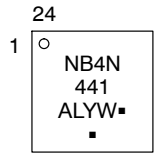
Description

The NB4N441 is a precision clock synthesizer which generates a differential LVPECL clock output frequency from 12.5 MHz to 425 MHz. A Serial Peripheral Interface (SPI) is used to configure the device to produce one of sixteen popular standard protocol output frequencies from a single 27 MHz crystal reference. The NB4N441 also has the added feature of allowing application specific output frequencies from 12.5 MHz to 425 MHz using crystals within the range of 10 MHz to 28 MHz.

Features

- Performs Precision Clock Generation and Synthesis from a Single 27 MHz Crystal Reference
- Serial Load Capability for Proprietary Frequencies
- Flexible Input Allows for External Clock Reference
- Exceeds Bellcore and ITU Jitter Generation Specification
- PLL Lock Detect Output
- Output Enable
- Fully Integrated Phase−Lock−Loop with Internal Loop Filter
- Operating Range: V_{CC} = 3.135 V to 3.465 V
- Small Footprint 24 Pin QFN
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NB4N441MNG	QFN−24 (Pb−Free)	92 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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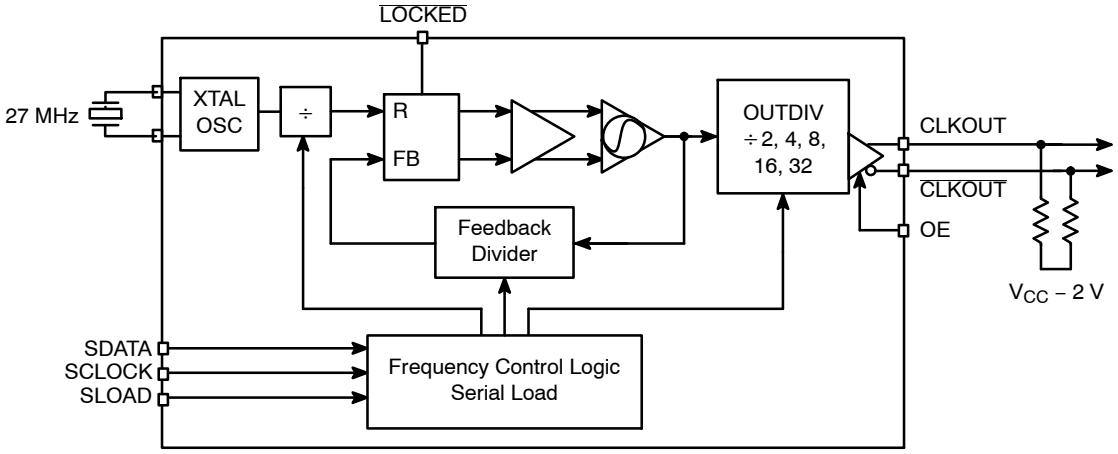


Figure 1. Simplified Block Diagram

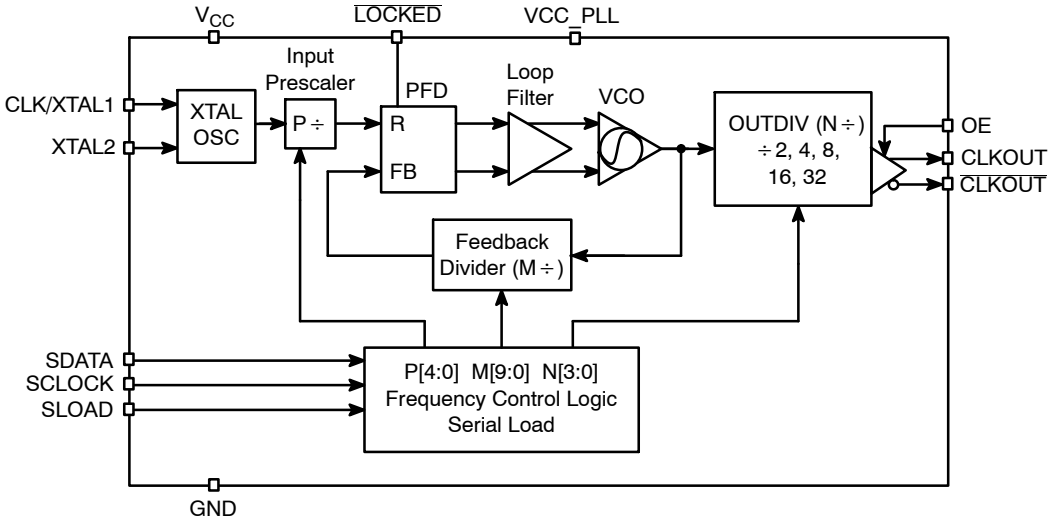


Figure 2. Block Diagram

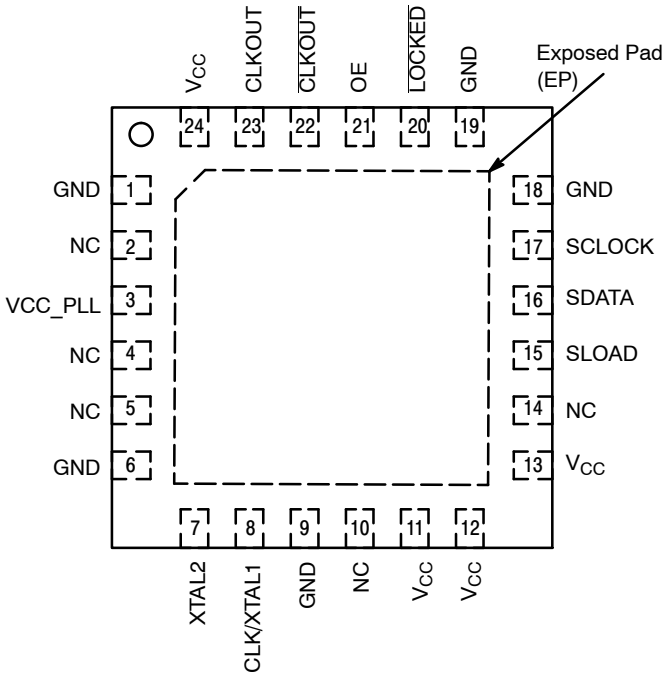


Figure 3. QFN−24 Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
11, 12, 13, 24	V_{CC}	Power Supply	Positive supply voltage.
3	VCC_PLL	PLL Power Supply	Positive supply voltage for the PLL.
1, 6, 9, 18, 19	GND	Ground	Ground.
20	$\overline{\text{LOCKED}}$	LVTTL Lock Output	When Low, this output provides indication that the PLL is locked and the device is in proper operating mode. When High, the PLL is out of lock.
2, 4, 5, 10, 14	NC		No Connect.
8	CLK / XTAL1,	LVTTL/LVCMOS Single Ended Clock or XTAL Inputs	The crystal is connected between the XTAL1 and XTAL2 pin. If driving single−ended, use XTAL1 and leave XTAL2 floating.
7	XTAL2		
15	SLOAD**	LVTTL / LVCMOS, Serial Load Input	Serial Load.
16	SDATA**	LVTTL / LVCMOS Serial Data Input	Serial Data Input.
17	SCLOCK**	LVTTL / LVCMOS Serial Clock Input	Serial Clock Input.
21	OE*	LVTTL Input	Synchronous Output Enable. When OE is HIGH or left OPEN, the outputs are enabled. When OE is LOW, the outputs are disabled.
22, 23	$\overline{\text{CLKOUT}}$ CLKOUT	LVPECL Output	Differential LVPECL Clock Outputs, Typically terminated with 50 Ω resistor to VCC − 2.0 V.
	EP		The Exposed Pad on the 24 pin QFN package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically connected to GND on the PC board.

*Pins will default HIGH when left Open
**Pins will default LOW when left Open

Table 2. STANDARD PROTOCOL / OUTPUT FREQUENCY SELECT TABLE WITH 27 MHz CRYSTAL REFERENCE

#	Protocol	CLKOUT (MHz)	Input Prescaler Divider P[4:0]	PLL FB Divider M[9:0]	Output Frequency Divider OUTDIV N[2:0]
0	OC−3 /STM−1	155.52	11001	1001000000	010
0	OC−12 / STM−4	155.52	11001	1001000000	010
0	OC−48 / STM−16	155.52	11001	1001000000	010
1	ETR	32	11011	1000000000	100
2	OC−1	51.84	11001	1100000000	100
3	Fast Ethernet	50	11011	1100100000	100
3	ESCON	50	11011	1100100000	100
4	FDDI	125	11011	0111110100	010
4	Infiniband	125	11011	0111110100	010
4	Gigabit Ethernet	125	11011	0111110100	010
4	PCIe	125	11011	0111110100	010
5	1/8 Fibre Channel	13.28125	11011	0110101001	101
6	1/4 Fibre Channel	26.5625	11011	1101010010	101
7	1/2 Fibre Channel	53.125	11011	1101010010	100
8	Fibre Channel	106.25	11011	1101010010	011
9	General	150	11011	1001011000	010
10	D1 Video	69	11011	1000101000	011
11	SONET Reference	19.44	11001	1001000000	101
12	2x Fibre Channel	212.5	11011	1101010010	010
13	4x Fibre Channel	425	11011	1101010010	001
14	XAUI	156.25	11011	1001110001	010
15	Serial ATA	100	11011	1100100000	011
16	HDTV	74.25	11011	1001010010	011
17	HDTV	148.50	11011	1001010010	010

Table 3. N−DIVIDER TABLE

N2	N1	N0	N Divider
0	0	0	na
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	na
1	1	1	na

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pullup Resistor	37.5kΩ
Internal Input Pulldown Resistor	75kΩ
ESD Protection Human Body Model Machine Model	 > 1000 V > 150 V
Moisture Sensitivity (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	2102
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.6	V
V_I	Input Voltage	GND = 0 V	GND = V_I = V_{CC}	3.6	V
I_{out}	LVPECL Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range	QFN−24		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−24 QFN−24		°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 3)	QFN−24		°C/W
T_{sol}	Wave Solder	< 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS V_{CC} = 3.135 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic		Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Loaded)		50	70	90	mA
I_{CCPLL}	PLL Power Supply Current		10	20	30	mA
V_{OH}	LVPECL Output HIGH Voltage (Notes 4 and 5)	V_{CC} = 3.3 V	V_{CC} − 1145 2155	V_{CC} − 1030 2270	V_{CC} − 895 2405	mV
V_{OL}	LVPECL Output LOW Voltage (Notes 4 and 5)	V_{CC} = 3.3 V	V_{CC} − 1945 1355	V_{CC} − 1760 1540	V_{CC} − 1695 1605	mV
V_{OHTTL}	Output HIGH Voltage ($\overline{\text{LOCKED}}$ Pin)	I_{OH} = −0.8 mA	2.5		V_{CC}	V
V_{OLTTL}	Output LOW Voltage ($\overline{\text{LOCKED}}$ Pin)		GND		0.4	V
V_{IH}	Input HIGH Voltage (LVTTL/LVCMOS)		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (LVTTL/LVCMOS)		GND		0.8	V
I_{IH}	Input HIGH Current, OE SCLK, SDATA, SLOAD OE, SCLK, SDATA, SLOAD	V_{IN} = 2.7 V, VCC_{max} V_{IN} = 2.7 V, VCC_{max} V_{IN} = V_{CC}, VCC_{max}	6.0 20 20		26 60 60	μA μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V, VCC_{max}			10	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. LVPECL Outputs loaded with 50 Ω termination resistors to V_{TT} = V_{CC} − 2.0 V for proper operation.
5. LVPECL Output parameters vary 1:1 with V_{CC}.

Table 7. AC CHARACTERISTICS V_{CC} = 3.135 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C (Note 6)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{IN}	Crystal Input Frequency External CLOCK Input Frequency (Pin 8) SCLOCK		10	27 27	28 50 10	MHz
V_{OUTPP}	Output Voltage Amplitude		600	800		mV
f_{VCO}	VCO Frequency Range		400		850	MHz
f_{CLKOUT}	Output Clock Frequency Range		12.5		425	MHz
t_{R}/t_{F_IN}	Input Clock Rise and Fall Time (CLK, Pin 8) (Note 7)				10	ns
t_{LOCK}	Maximum PLL Lock Time			0.5	5	ms
DCO	Output CLOCK Duty Cycle (Differential Configuration)		48		52	%
$t_{JITTER(pd)}$	Period Jitter (RMS, 1σ, 10,000 Cycles) (Notes 8 and 9)			3.5	6.5	ps
$t_{JITTER(pd)}$	Period Jitter (Peak−to−Peak, 10,000 Cycles) (Note 9)			25	40	ps
t_s	Setup Time	SDATA to SCLOCK SCLOCK to SLOAD	20 20			ns ns
t_h	Hold Time	SDATA to SCLOCK SCLOCK to SLOAD	20 20			ns ns
t_{pwmin}	Minimum Pulse Width SLOAD		20			ns
t_r, t_f	Output Rise/Fall Times (Note 7) CLKOUT / $\overline{\text{CLKOUT}}$		175	300	425	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. LVPECL Outputs loaded with 50 Ω to V_{CC} − 2.0 V.
7. Measured 20% to 80%
8. Additive RMS jitter with 50% duty cycle input clock signal at 27.000 MHz; f_{OUT} = 155 MHz.
9. f_{OUT} = 155 MHz. Protocol 13.28125 MHz will have typical period jitter (RMS) of 14 ps and a typical cycle−to−cycle jitter of 95 ps.

APPLICATIONS INFORMATION

General

The NB4N441 is a precision clock synthesizer which generates a differential LVPECL clock output frequency from 12.5 MHz to 425 MHz. A three−wire SPI interface is used to configure the device to produce the exact frequency of one of sixteen predefined popular standard protocol output frequencies from a single 27 MHz crystal reference; see Table 1. This serial interface gives the user complete control of each internal counter/divider.

If a different or custom output frequency is required, the SPI interface can also enable the user to configure the device for frequencies not specified in Table 1.

Input Clock / Crystal Functionality

To generate the exact protocol frequencies in Table 1, a 27.000 MHz frequency source is required. This can be accomplished by connecting a 27.000 MHz crystal across the XTAL1 and XTAL2 pins. If driving single ended, use the XTAL1 pin and leave XTAL2 floating. The CLK/XTAL1 input will accept a LVTTL/LVCMOS input.

Frequency Control Logic Configuration

The NB4N441 includes a 5−bit input prescaler, a 10−bit divider for the PLL feedback path and a 3−bit Output Divider, which divides the VCO frequency by 2, 4, 8, 16, or 32. The Frequency Control Logic for the NB4N441 configures these dividers and counters through the Serial inputs and will select one of the sixteen predetermined clock frequencies in Table 1. The serial interface can also be used to configure the device for user specified custom frequencies not specified in Table 1. Output frequencies are generated based on the following equation: $F_{OUT} = (F_{xtal}/P) * M \div N$, with the stipulation that the internal VCO frequency be $400\ MHz < VCO < 850\ MHz$ with $VCO = F_{OUT} * N$ and $10\ MHz < F_{xtal} < 28\ MHz$.

Output Enable

The NB4N441 incorporates a synchronous output Disable/Enable pin, OE. The synchronous output enable pin insures no runt clock pulses are generated. When disabled, CLKOUT is set LOW and $\overline{CLKOUT}$ is set HIGH.

Table 8. Table 8. Output Enable Function

OE	Function
1	Clock Outputs Enabled
0	Clock Outputs Disabled CLKOUT = L, $\overline{CLKOUT}$ = H

Lock Detect Functionality

The NB4N441 features a PLL Lock Detect function which indicates the locked status of the PLL. When the PLL is locked, the $\overline{LOCKED}$ output pin asserts a logic Low. When the internal phase lock is lost (such as when the input clock stops, drifts beyond the pullable range of the crystal, or suddenly shifts in phase), the $\overline{LOCKED}$ output goes High.

Table 9. Table 9. Lock Detect Function

$\overline{LOCKED}$	Function
0	PLL is Locked
1	PLL is not Locked

Using the On−Board Crystal Oscillator

The NB4N441 features a fully integrated on−board crystal oscillator to minimize system implementation costs.

The crystal should be fundamental mode, parallel resonant. For exact tuning of cyrstal frequency, capacitors should be connected from pins X1 and X2. Typical loading should be on the order of 20 pF to 30 pF (on each crystal input pin). As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NB4N441 as possible to avoid any board level parasitic effects. To facilitate collocation, surface mount crystals are recommended, but not required.

Table 10. CRYSTAL SPECIFICATIONS

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Load Capacitance	18 pF
Frequency Tolerance	±15 ppm at 25°C
Frequency/Temperature Stability	±20 ppm 0 to 70°C
Operating Range	0 to 70°C or −40 to +85°C
Shunt Capacitance	5 pF Max
Equivalent Series Resistance (ESR)	50 Ω Max
Correlation Drive Level	1.0 μW Max
Aging	5 ppm / Yr (First 3 Years) 15 ppm /10 Yrs

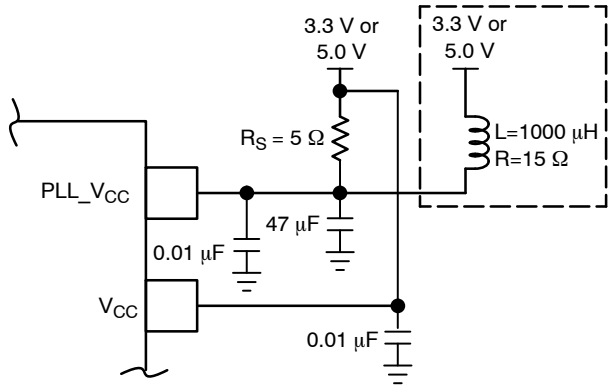


Figure 4. Power Supply Filter

Power Supply Filtering

The NB4N441 is a mixed analog/digital product and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The NB4N441 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_V_{CC}) of the device. The purpose of this design technique is to try and isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase−locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_V_{CC} Pin for the NB4N441. Figure 4 illustrates a typical power supply filter scheme. The NB4N441 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_V_{CC} pin of the NB4N441. From the data sheet, the PLL_V_{CC} current (the current sourced through the PLL_V_{CC} Pin) is typically 26 mA. Assuming that a minimum of 2.9 V must be maintained on the PLL_V_{CC} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of 5 Ω Max to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. The level of required filtering is subject to further optimization and simplification. All the V_{CC} pins are connected to the same V_{CC} plane. All the ground pins (GND) are connected to the same GND plane.

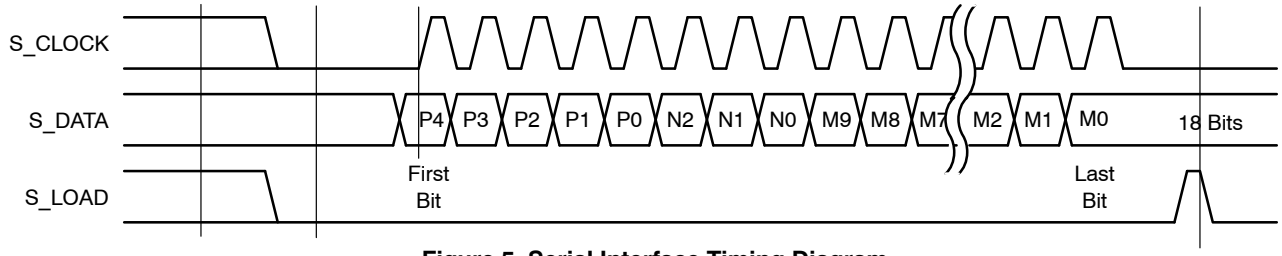


Figure 5. Serial Interface Timing Diagram

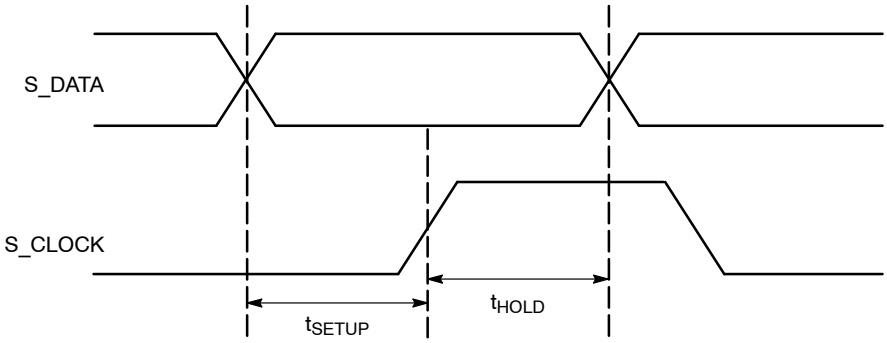


Figure 6. Setup and Hold

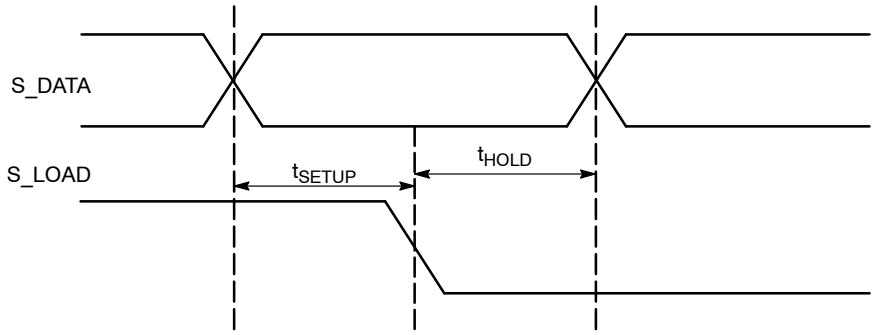


Figure 7. Setup and Hold

Jitter Performance

Jitter is a common parameter associated with clock generation and distribution. Clock jitter can be defined as the deviation in a clock's output transition from its ideal position.

Cycle−to−Cycle Jitter (short−term) is the period variation between two adjacent cycles over a defined number of observed cycles. The number of cycles observed is application dependent but the JEDEC specification is 1000 cycles.

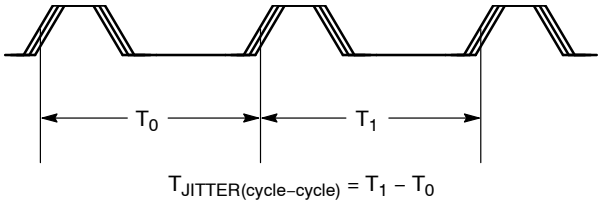


Figure 8. Cycle−to−Cycle Jitter

Peak−to−Peak Jitter is the difference between the highest and lowest acquired value and is represented as the width of the Gaussian base.

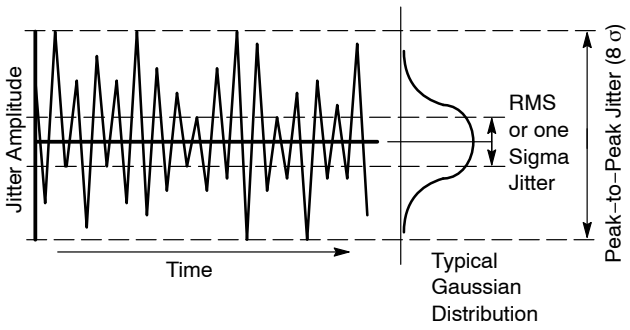


Figure 9. Peak−to−Peak Jitter

There are different ways to measure jitter and often they are confused with one another. The typical method of measuring jitter is to look at the timing signal with an oscilloscope and observe the variations in period−to−period or cycle−to−cycle. If the scope is set up to trigger on every rising or falling edge, set to infinite persistence mode and allowed to trace sufficient cycles, it is possible to determine the maximum and minimum periods of the timing signal. Digital scopes can accumulate a large number of cycles, create a histogram of the edge placements and record peak−to−peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. These scopes can also store a finite number of period durations and post−processing software can analyze the data to find the maximum and minimum periods.

Recent hardware and software developments have resulted in advanced jitter measurement techniques. The Tektronix TDS−series oscilloscopes have superb jitter analysis capabilities on non−contiguous clocks with their histogram and statistics capabilities. The Tektronix TDSJIT2/3 Jitter Analysis software provides many key timing parameter measurements and will extend that capability by making jitter measurements on contiguous clock and data cycles from single−shot acquisitions.

M1 by Amherst was used as well and both test methods correlated.

Long−Term Period Jitter is the maximum jitter observed at the end of a period's edge when compared to the position of the perfect reference clock's edge and is specified by the number of cycles over which the jitter is measured. The number of cycles used to look for the maximum jitter varies by application but the JEDEC spec is 10,000 observed cycles.

The NBC4N441 exhibit long term and cycle−to−cycle jitter, which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility associated with a synthesizer over a fixed frequency oscillator. The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

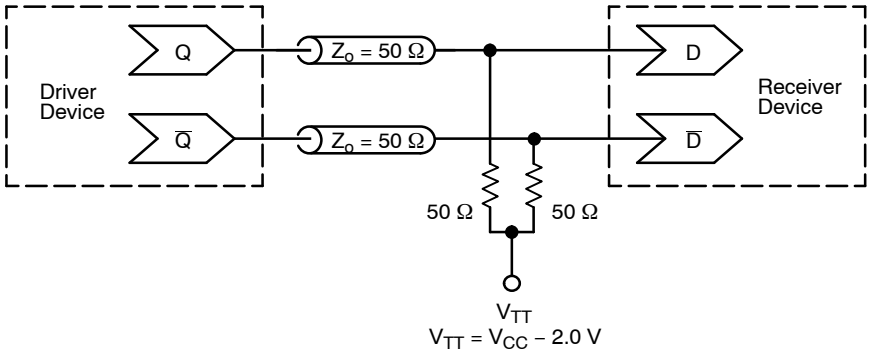


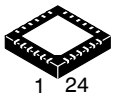
Figure 10. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D − Termination of ECL Logic Devices.)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

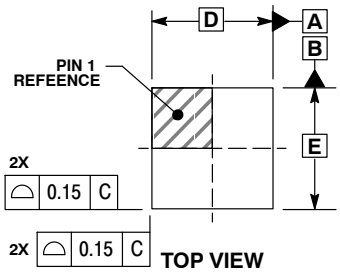
ON Semiconductor®

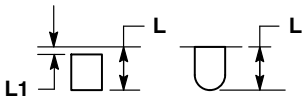
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

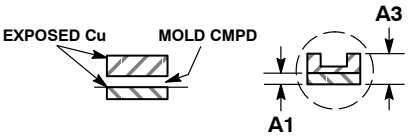
DATE 05 JUN 2012

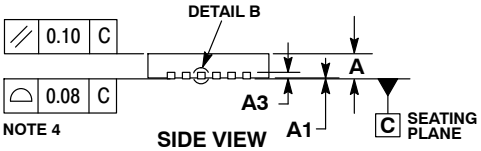


SCALE 2:1



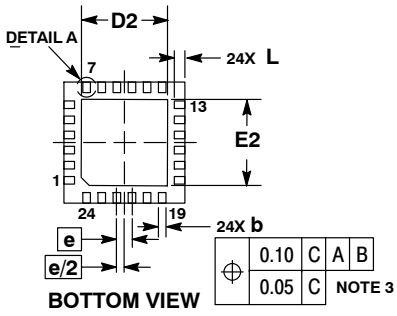






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15



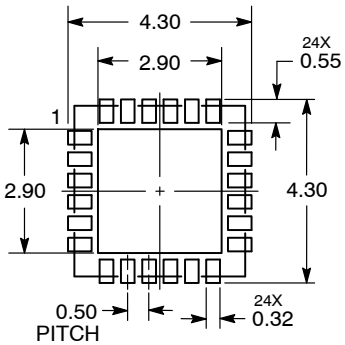
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT



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DESCRIPTION:	**QFN24, 4X4, 0.5P**		**PAGE 1 OF 1**

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