Double Hex Driver

NCV7708F

The NCV7708F is a fully protected Hex Half Bridge Driver designed specifically for automotive and industrial motion control applications. The six low and high side drivers are freely configurable and can be controlled separately. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard SPI interface.

Features

- Ultra Low Quiescent Current Sleep Mode
- Six Independent High−Side and Six independent Low−Side Drivers
- Integrated Freewheeling Protection (LS and HS)
- Internal Upper and Lower Clamp Diodes
- Configurable as H−Bridge Drivers
- $R_{DS(on)}$ = 0.6 Ω (typ)
- 5 MHz SPI Control
- SPI Valid Frame Detection
- Compliance with 5 V and 3.3 V Systems
- Overvoltage Lockout
- Undervoltage Lockout
- Fault Reporting
- Current Limit
- Overtemperature Protection
- Internally Fused Lead in SOIC−28
- SSOP−24 NB EPAD
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management

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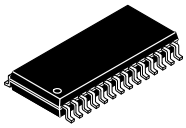
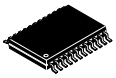
MARKING DIAGRAMS



SOIC−28
DW SUFFIX
CASE 751F



SSOP−24 NB EP
DQ SUFFIX
CASE 940AK

X	= Optional Wafer Fab Indicator
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7708FDWR2G*	SOIC−28W (Pb−Free)	1000 / Tape & Reel
NCV7708FDQR2G	SSOP−24N (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact your local sales representative for the NCV7708F device availability in SOIC−28 package.

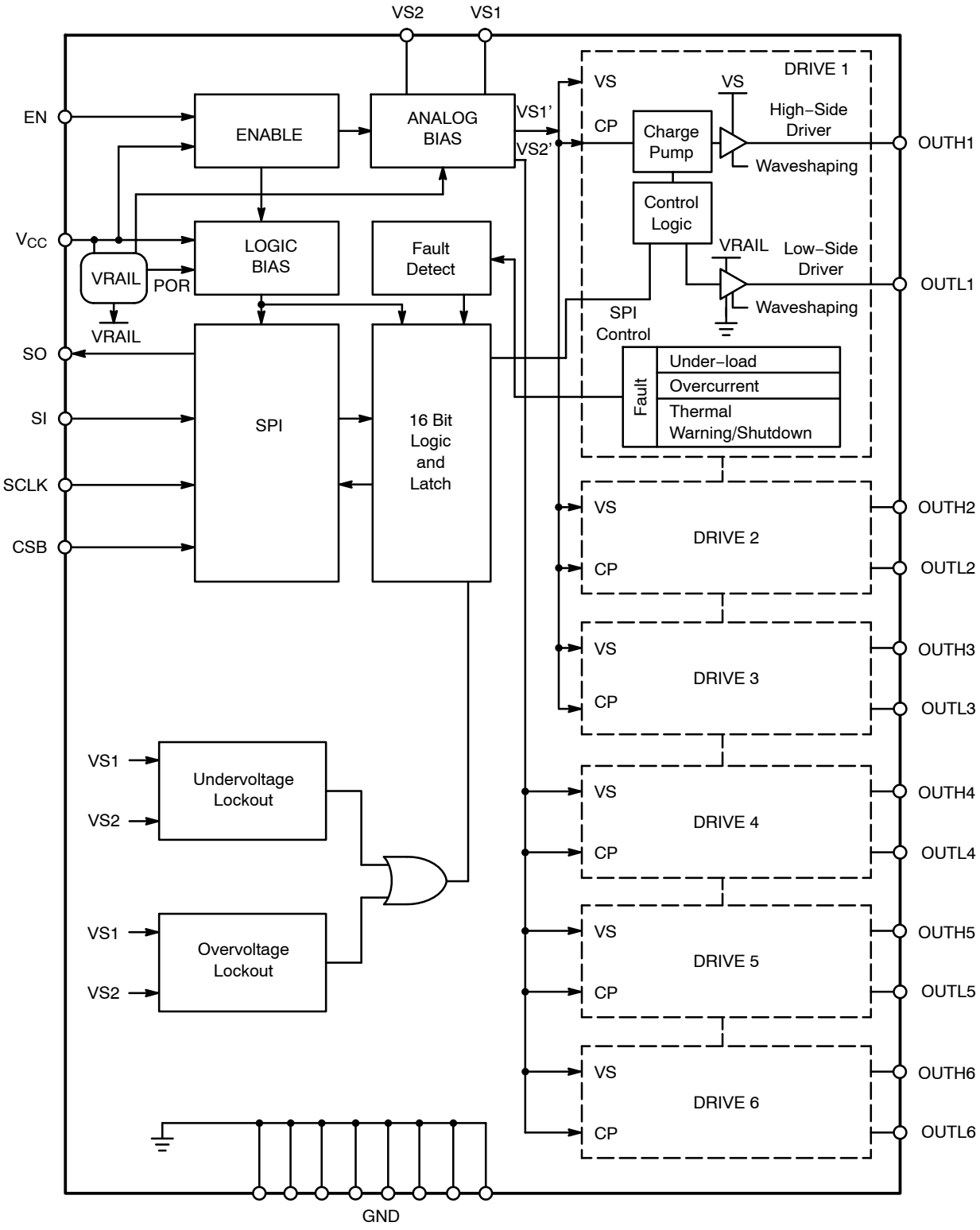


Figure 1. Block Diagram

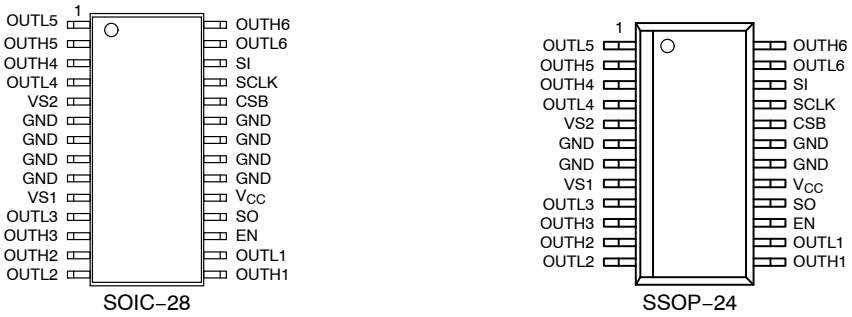


Figure 2. Pin Connection

PIN DESCRIPTION

Pin No.		Symbol	Description
SSOP−24	SOIC−28		
1	1	OUTL5	Output Low Side 5. Open drain output driver with internal reverse diode.
2	2	OUTH5	Output High Side 5. Open source output driver with internal reverse diode. Drain connected to VS2'.
3	3	OUTH4	Output High Side 4. Open source output driver with internal reverse diode. Drain connected to VS2'.
4	4	OUTL4	Output Low Side 4. Open drain output driver with internal reverse diode.
5	5	VS2	Power Supply input for the High−Side Output Drivers 4, 5, and 6.
6	6	GND	Ground
7	7	GND	Ground
–	8	GND	Ground
–	9	GND	Ground
8	10	VS1	Power Supply input for the High−Side Output Drivers 1, 2, and 3
9	11	OUTL3	Output Low Side 3. Open drain output driver with internal reverse diode.
10	12	OUTH3	Output High Side 3. Open source output driver with internal reverse diode. Drain connected to VS1'.
11	13	OUTH2	Output High Side 2. Open source output driver with internal reverse diode. Drain connected to VS1'.
12	14	OUTL2	Output Low Side 2. Open drain output driver with internal reverse diode.
13	15	OUTH1	Output High Side 1. Open source output driver with internal reverse diode. Drain connected to VS1'.
14	16	OUTL1	Output Low Side 1. Open drain output driver with internal reverse diode.
15	17	EN	Enable. Input high wakes the IC up from sleep mode.
16	18	SO	Serial Output. 16 bit serial communications output.
17	19	V_{CC}	Power supply input for Logic.
18	20	GND	Ground
19	21	GND	Ground
–	22	GND	Ground
–	23	GND	Ground
20	24	CSB	Chip Select Bar. Active low serial port operation.
21	25	SCLK	Serial Clock. Clock input for use with SPI communication.
22	26	SI	Serial Input. 16 bit serial communications input.
23	27	OUTL6	Output Low Side 6. Open drain output driver with internal reverse diode.
24	28	OUTH6	Output High Side 6. Open source output driver with internal reverse diode. Drain connected to VS2'.
EPAD	–	EPAD	Connect to Ground for best thermal performance or leave unconnected.

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 −0.3 to 40 −1.0	V
Output Pin OUTHx (DC) (AC − inductive clamping)	 −0.3 to 40 −8.0	V
Output Pin OUTLx (DC) (AC), t < 500 ms, IOUTLx > −2 A (AC Inductive Clamping)	 −0.3 to 36 −1.0 45	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	−0.3 to 5.5	V
Output Current (OUTL1, OUTL2, OUTL3, OUTL4, OUTL5, OUTL6, OUTH1, OUTH2, OUTH3, OUTH4, OUTH5, OUTH6) (DC) Vds = 12 V (DC) Vds = 20 V (DC) Vds = 40 V (AC) Vds = 12 V, (50 ms pulse, 1 s period) (AC) Vds = 20 V, (50 ms pulse, 1 s period) (AC) Vds = 40 V, (50 ms pulse, 1 s period)	 −1.5 to 1.5 −0.7 to 0.7 −0.25 to 0.25 −2.0 to 2.0 −0.9 to 0.9 −0.3 to 0.3	A
Electrostatic Discharge, Human Body Model, VS1, VS2, OUTx (Note 1)	4.0	kV
Electrostatic Discharge, Human Body Model, all other pins	2.0	kV
Electrostatic Discharge, Machine Model	200	V
Electrostatic Discharge, Charged Device Model	1.0	kV
Short Circuit Reliability Characterization (AEC−Q10x)	GRADE A	−
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−55 to 150	°C
Moisture Sensitivity Level SOIC−28 SSOP−24 EPAD	MSL 3 MSL 2	−
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C (Note 2)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested with a VS1/VS2 power supply common point.
2. For additional information, please see or download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CONDITIONS

Thermal Parameters	Test Conditions, Typical Value		Unit
	Board Details (Note 3)	Board Details (Note 4)	
SOIC−28			
Junction−to−Lead (psi−JL8, Ψ_{JL8}) or Pins 6−9, 20−23	10	11	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	78	63	°C/W
SSOP−24 EPAD			
Junction−to−Board ($R_{\Psi B}$)	−	2	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	−	54	°C/W
Junction−to−Lead ($R_{\Psi JL}$)	−	7	°C/W

3. 1−oz copper, 240 mm^2 copper area, 0.062″ thick FR4. This is the minimum pad board size.
4. 1−oz copper, 986 mm^2 copper area, 0.062″ thick FR4.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value		Unit
		Min	Max	
Digital Supply Input Voltage (V_{CC})	V_{CCmax}	3.15	5.25	V
Battery Supply Input Voltage (V_S)	V_{Smax}	5.5	28	V
DC Output Current (I(OUTLx), I(OUTHx))	DC_{max}	–	0.5	A
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
GENERAL						
Supply Current (VS1 + VS2) Sleep Mode (Note 5)	I_{vs_sleep}	VS1 = VS2 = 13.2 V, V_{CC} = CSB = 5 V, EN = SI = SCLK = 0 V (−40°C to 85°C)	–	1.0	2.5	μA
Supply Current (VS1) Active Mode	I_{vs1_act}	EN = V_{CC}, 5.5 V < VSx < 35 V No Load	–	1.25	2.5	mA
Supply Current (V_{CC}) − Sleep Mode (Note 5)	I_{vcc_sleep}	CSB = V_{CC}, EN = SI = SCLK = 0 V (−40°C to 85°C)	–	1.0	2.5	μA
Supply Current (V_{CC}) − Active Mode	I_{vcc_act}	EN = CSB = V_{CC}, SI = SCLK = 0 V	–	1.5	3.0	mA
Supply Current (VS2) Active Mode	I_{vs2_act}	EN = V_{CC}, 5.5 V < VSx < 35 V No Load	–	1.25	2.5	mA
V_{CC} Power−On−Reset Threshold	V_{CCpor}		–	2.55	2.9	V
VSx Undervoltage Detection Threshold	V_{Suv}	VSx decreasing	3.7	4.1	4.5	V
VSx Undervoltage Detection Hysteresis	V_{Suv_hys}		100	365	450	mV
VSx Overvoltage Detection Threshold	V_{Sov}	VSx increasing	33	36.5	40.0	V
VSx Overvoltage Detection Hysteresis	V_{Sov_hys}		1	2.5	4.0	V
Thermal Warning (Note 6)	T_{tw}		120	140	170	°C
Thermal Warning Hysteresis (Note 6)	T_{tw_hys}		–	20	–	°C
Thermal Shutdown (Note 6)	T_{tsd}		155	175	195	°C
Ratio of Thermal Shutdown to Thermal Warning (Note 6)	T_{tsd}/T_{tw}		1.05	1.20	–	–
OUTPUTS						
Output High $R_{DS(on)}$ (source and sink)	R_{DSon_src} R_{DSon_snk}	I_{out} = −500 mA 25°C −40°C < T_J < 150°C	 – –	 0.6 –	 1.3 1.7	Ω
Source Leakage Current	I_{src}	OUTH(1−6) = 0 V, Vsx = 40 V, V_{CC} = 5 V OUTH(1−6) = 0 V, Vsx = 13.2 V, V_{CC} = 5V	−5.0 −1.0	– –	– –	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. For temperatures above 85°C, refer to graphs for VSx and V_{CC} Sleep Current vs. Temperature on page 17.
6. Thermal characteristics are not subject to production test.
7. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 17.
8. Current limit is active with and without overcurrent detection.
9. Not production tested.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUTS						
Sink Leakage Current	I_{snk}	OUTL(1−6) = 34 V, V_{CC} = 5 V OUTL(1−6) = 34 V, V_{CC} = 5 V, T = 25°C	− −	− −	5.0 1.0	μA
Power Transistor Body Diode Forward Voltage	V_{bd_fwd}	I_F = 500 mA	−	0.9	1.3	V
High−Side Clamping Voltage (Note 7)	V_{clp_hs}	$I_{(OUTHx)}$ = −50 mA	−	−	−0.7	V
Low−Side Clamping Voltage	V_{clp_ls}	$I_{(OUTLx)}$ = 50 mA	36	−	45	V
UNDER LOAD						
Under Load Detection Threshold (OUTLx)	I_{ul_ls}	V_{CC} = 5 V, Vsx = 13.2 V	2.0	8.0	16	mA
Under Load Detection Threshold (OUTHx)	I_{ul_hs}	V_{CC} = 5 V, Vsx = 13.2 V	−16	−8.0	−2.0	mA
Under Load Detection Delay Time	t_{ul_del}	V_{CC} = 5 V, Vsx = 13.2 V	200	350	600	μs
OVERCURRENT						
Overcurrent Shutdown Threshold (OUTHx)	I_{ocsd_hs}	V_{CC} = 5 V, Vsx = 13.2 V, Bit13 = 1	−2.0	−1.45	−1.1	A
Overcurrent Shutdown Threshold (OUTLx)	I_{ocsd_ls}	V_{CC} = 5 V, Vsx = 13.2 V, Bit13 = 1	1.1	1.45	2.0	A
Overcurrent Shutdown Delay Time	t_{ocsd_0} t_{ocsd_1}	V_{CC} = 5 V, Vsx = 13.2 V, Bit13 = 0 Bit13 = 1	80 10	200 25	400 50	μs μs
CURRENT LIMIT (Note 8)						
Current Limit (OUTHx)	I_{lim_hs}	V_{CC} = 5 V, Vsx = 13.2 V	−5.0	−3.0	−2.0	A
Current Limit (OUTLx)	I_{lim_ls}	V_{CC} = 5 V, Vsx = 13.2 V	2.0	3.0	5.0	A
LOGIC INPUTS (EN, SI, SCLK, CSB)						
Input Threshold − High − Low	V_{inth}		2.0 −	− −	− 0.8	V
Input Hysteresis (SI, SCLK, CSB)	V_{inhys_spi}		100	300	600	mV
Input Hysteresis (EN)	V_{inhys_en}		100	400	800	mV
Pull−down Resistance (EN, SI, SCLK)	R_{pd}	EN = SI = SCLK = V_{CC}	50	125	250	kΩ
Pull−up Resistance (CSB)	R_{pu}	CSB = 0 V	50	125	250	kΩ
Input Capacitance (Note 9)	C_{IN}		−	10	15	pF
LOGIC OUTPUT (SO)						
Output High	V_{soh}	I_{out} = 1 mA	V_{CC} − 1.0	V_{CC} − 0.7	−	V
Output Low	V_{sol}	I_{out} = −1.6 mA	−	0.2	0.4	V
Tri−state Leakage	I_{so}	CSB = V_{CC}, 0 V < SO < V_{CC}	−10	−	10	μA
Tri−state Input Capacitance (Note 9)	C_{so}	CSB = V_{CC}, 0 V < V_{CC} < 5.25 V	−	10	15	pF
TIMING SPECIFICATIONS						
High Side Turn On Time	t_{hson}	Vs = 13.2 V, R_{load} = 25 Ω	−	7.5	13	μs
High Side Turn Off Time	t_{hsoff}	Vs = 13.2 V, R_{load} = 25 Ω	−	3.0	6.0	μs
Low Side Turn On Time	t_{lson}	Vs = 13.2 V, R_{load} = 25 Ω	−	6.5	13	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. For temperatures above 85°C, refer to graphs for VSx and V_{CC} Sleep Current vs. Temperature on page 17.
6. Thermal characteristics are not subject to production test.
7. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 17.
8. Current limit is active with and without overcurrent detection.
9. Not production tested.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
TIMING SPECIFICATIONS						
Low Side Turn Off Time	t_{lsoff}	Vs = 13.2 V, R_{load} = 25 Ω	–	2.0	5.0	μs
High Side Rise Time	t_{hsr}	Vs = 13.2 V, R_{load} = 25 Ω	–	4.0	8.0	μs
High Side Fall Time	t_{hsf}	Vs = 13.2 V, R_{load} = 25 Ω	–	2.0	3.0	μs
Low Side Rise Time	t_{lsr}	Vs = 13.2 V, R_{load} = 25 Ω	–	1.0	2.0	μs
Low Side Fall Time	t_{lsf}	Vs = 13.2 V, R_{load} = 25 Ω	–	1.0	3.0	μs
Non−Overlap Time	$t_{hsOfflsOn}$	High Side Turn Off To Low Side Turn On	1.5	–	–	μs
Non−Overlap Time	$t_{lsOffhsOn}$	Low Side Turn Off To High Side Turn On	1.5	–	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. For temperatures above 85°C, refer to graphs for VSx and V_{CC} Sleep Current vs. Temperature on page 17.
6. Thermal characteristics are not subject to production test.
7. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 17.
8. Current limit is active with and without overcurrent detection.
9. Not production tested.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, EN = V_{CC} = 5 V, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE (V_{CC} = 5 V)						
SCLK Frequency		f_{SCLK}	–	–	5.0	MHz
SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V	t_{SCLK}	200 500	– –	– –	ns
SCLK High Time		t_{CLKH}	85	–	–	ns
SCLK Low Time		t_{CLKL}	85	–	–	ns
SCLK Setup Time		t_{CLKSU1} t_{CLKSU2}	85 85	– –	– –	ns
SI Setup Time		t_{SISU}	50	–	–	ns
SI Hold Time		t_{SIHT}	50	–	–	ns
CSB Setup Time		t_{CSBSU1} t_{CSBSU2}	100 100	– –	– –	ns
CSB High Time (Note 10)		t_{CSBHT}	5.0	–	–	μs
SO enable after CSB falling edge		t_{SOCSBF}	–	–	200	ns
SO disable after CSB rising edge		t_{SOCSBR}	–	–	200	ns
SO Rise Time (10% to 90%)	C_{load} = 40 pF	t_{SORISE}	–	10	25	ns
SO Fall Time (90% to 10%)	C_{load} = 40 pF	t_{SOFALL}	–	10	25	ns
SO Valid Time (Note 11)	SCLK High to SO 50%	t_{SOV}	–	50	100	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. This is the minimum time the user must wait between SPI commands.
11. Not tested in production

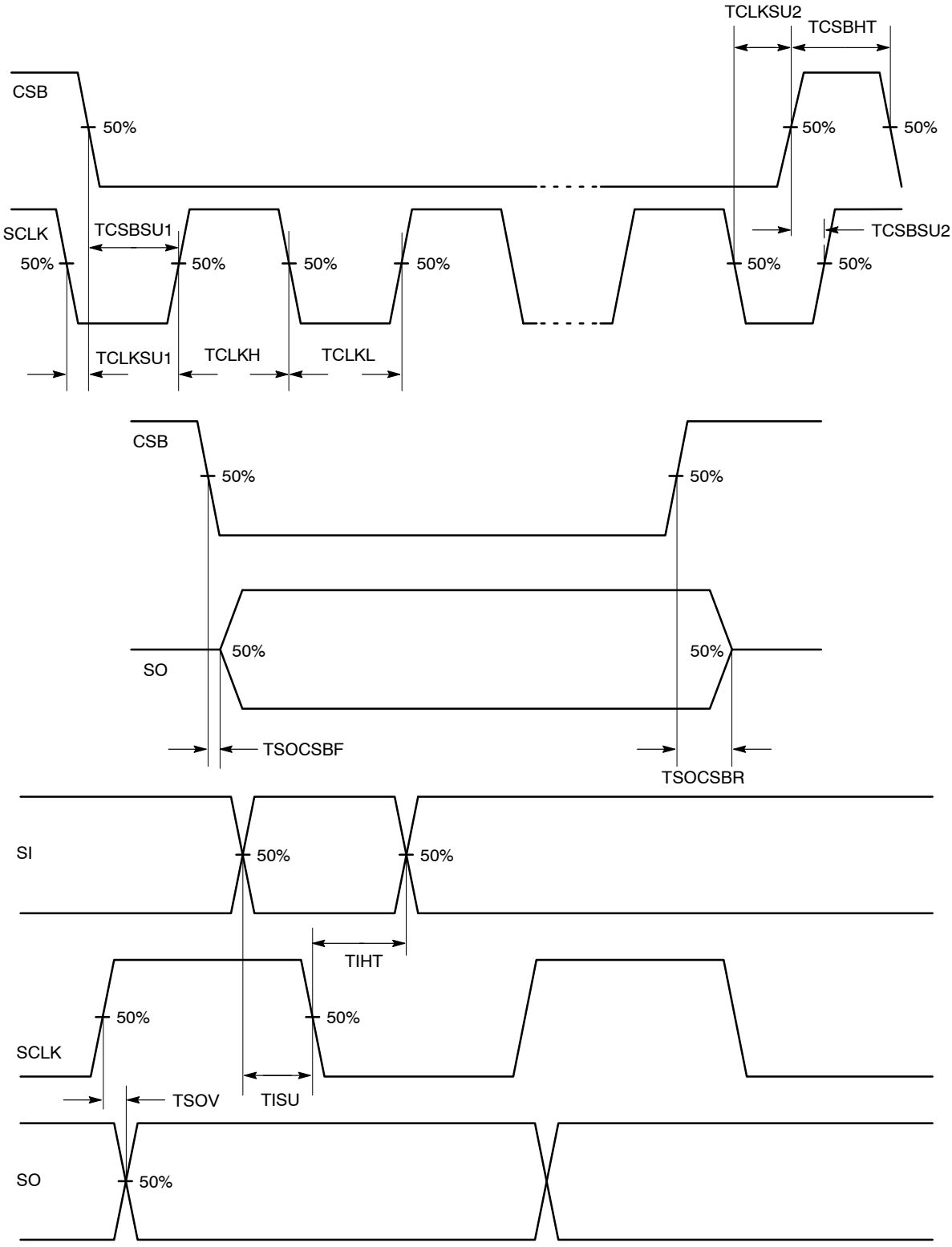


Figure 3. SPI Timing Diagram

SPI Communication

Standard 16−bit communication has been implemented for the communication of this IC to turn drivers on and off, and to report faults. (Reference the SPI Communication Frame Format Diagram). The LSB (Least Significant Bit) is clocked in first.

For SPI communication, the device must first be enabled (EN = high). The SPI inputs are TTL compatible and the SO output high level is defined by the applied VCC. The active-low CSB input has a pull−up resistor. SPI communication is active when CSB is low. Providing a pull-up resistor insures the communication bus is not active should the communication link between the microcontroller and NCV7708F become open. SCLK and SI have pull−down resistors. This provides known states when the SPI is not active.

Communication is implemented as follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (serial input) pin. The SI input signal is latched on the falling edge of SCLK.
3. Current SO data is simultaneously shifted out on every rising edge of SCLK starting with the LSB (TW).
4. CSB goes high to transfer the clocked in information to the data registers.
   (Note: SO is tristate when CSB is high.)
5. The SI data will be accepted when a valid SPI frame is detected. A valid SPI frame consists of the above conditions and a complete set of multiples of 16 bit words. Invalid frames are ignored with previous input data intact.

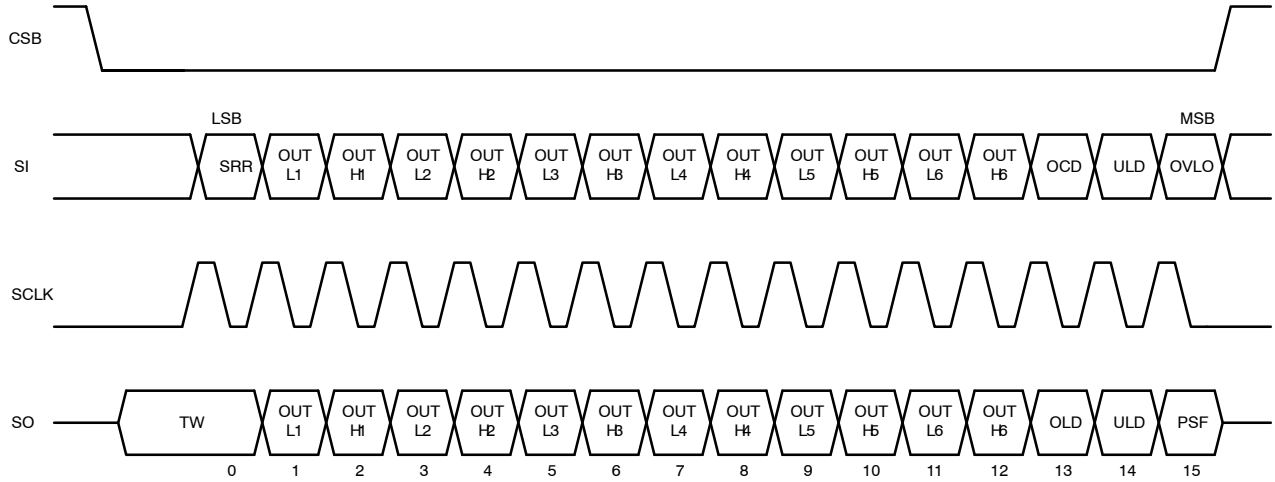


Figure 4. SPI Communication Frame Format

The table below defines the programming bits and diagnostic bits. Fault information is sequentially clocked out the SO pin of the NCV7708F as programming information is clocked into the SI pin of the device. Daisy chain communication between SPI compatible IC's is possible by connection of the serial output pin (SO) to the input of the sequential IC (SI).

Input Data		
Bit #	**Bit Description**	**Bit Status**
15	Overvoltage Lock Out Control (OVLO)	0 = Disable
		1 = Enable
14	Under Load Detection Shut Down Control (ULD)	0 = Disable
		1 = Enable
13	Overcurrent Detection Shut Down Control (OCD)	0 = 200 μsec
		1 = 25 μsec
12	OUTH6	0 = Off
		1 = On
11	OUTL6	0 = Off
		1 = On
10	OUTH5	0 = Off
		1 = On
9	OUTL5	0 = Off
		1 = On
8	OUTH4	0 = Off
		1 = On
7	OUTL4	0 = Off
		1 = On
6	OUTH3	0 = Off
		1 = On
5	OUTL3	0 = Off
		1 = On
4	OUTH2	0 = Off
		1 = On
3	OUTL2	0 = Off
		1 = On
2	OUTH1	0 = Off
		1 = On
1	OUTL1	0 = Off
		1 = On
0	Status Register Reset (SRR)	0 = No Reset
		1 = Reset

*Output Bits [1:12] represent the state of the designated outputs.

Output Data		
Bit #	**Bit Description**	**Bit Status**
15	Power Supply Fail Signal (OVLO or UVLO = PSF)	0 = No Fault
		1 = Fault
14	Under Load Detect Signal (ULD)	0 = No Fault
		1 = Fault
13	Over Load Detect Signal (OLD)	0 = No Fault
		1 = Fault
12	OUTH6*	0 = Off
		1 = On
11	OUTL6*	0 = Off
		1 = On
10	OUTH5*	0 = Off
		1 = On
9	OUTL5*	0 = Off
		1 = On
8	OUTH4*	0 = Off
		1 = On
7	OUTL4*	0 = Off
		1 = On
6	OUTH3*	0 = Off
		1 = On
5	OUTL3*	0 = Off
		1 = On
4	OUTH2*	0 = Off
		1 = On
3	OUTL2*	0 = Off
		1 = On
2	OUTH1*	0 = Off
		1 = On
1	OUTL1*	0 = Off
		1 = On
0	Thermal Warning (TW)	0 = Not in TW
		1 = In TW

Status Register Reset – SRR

Sending SRR = 1 clears status memory and reactivates faulted output. The previous SI data pattern must be sent with SRR to preserve device configuration and output states. SRR takes effect at the rising edge of CSB. If a fault is still present when SRR is sent, protection can be re−engaged and shutdown can recur. The device can also be reset by toggling the EN pin or by VCC power-on reset.

When asserted, all latched faults are cleared (TW, OLD, ULD, and PSF).

CHARACTERISTIC TIMING DIAGRAMS

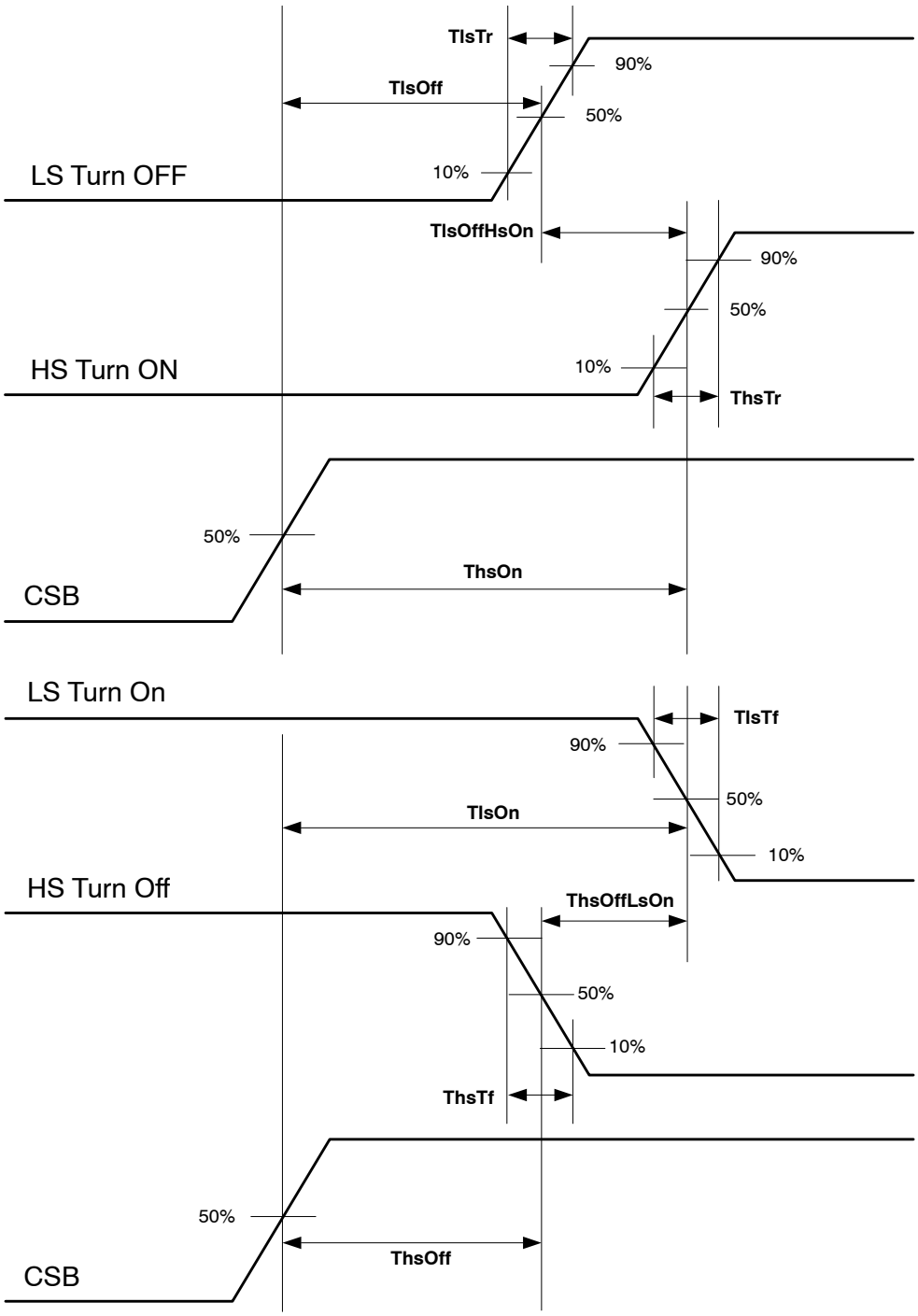


Figure 5. Detailed Driver Timing

DETAILED OPERATING DESCRIPTION

General

The NCV7708F Double Hex Driver provides drive capability for three independent H−Bridge configurations, or 6 High Side configurations with 6 Low Side configurations, or any combination of arrangements. Each output drive is characterized for a 500 mA load and has a typical 1.0 A surge capability (at 13.2 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

Sleep Mode

An Enable function (EN = Low) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode.

Input Impedance

A pull down resistor is provided on the EN input to ensure the device is off if the input signal is lost. Pull down resistors are also provided on the SI and SCLK inputs. A pull up resistor is provided for the CSB input for the same reason. A loss of signal pulls the CSB input high to stop any spurious signals into the SPI port.

Power Up/Down Control

An undervoltage lockout circuit prevents the output drivers from turning on unintentionally. This control is provided by monitoring the voltages on the VS1, VS2, and V_{CC} pins. Each analog power pin (VS1 or VS2) powers their respective high−side output drivers and supporting charge pump. VS1 powers OUTH1, OUTH2, and OUTH3. VS2 powers OUTH4, OUTH5, and OUTH6.

All low−side drivers are powered by VRAIL via V_{CC}.

All drivers are initialized in the off (high impedance) condition. Power up sequencing of V_{CC}, VS1, and VS2 is up to the user. The voltage on VS1 and VS2 should be operated at the same potential. If the VSx supply moves into either of the VS under voltage or overvoltage regions (with (OVLO = 1), the output drivers are switched to high Z, but command and status data is preserved.

Internal power−up circuitry on the logic supply pin supports a smooth turn on transition. V_{CC} power up resets the internal logic such that all output drivers will be off as power is applied. Exceeding the under voltage lockout threshold on V_{CC} allows information to be input through the SPI port for turn on control. Logic information remains intact over the entire VS1 and VS2 voltage range.

Current Limit

OUTx current is limited per the Current Limit electrical parameter for each driver. The magnitude of the current has a minimum specification of 2 A at V_{CC} = 5 V and Vsx = 13.2 V. The output is protected for high power conditions during Current Limit by thermal shutdown and the Overcurrent Detection shutdown function. Overcurrent Detection shutdown protects the device during current limit because the Overcurrent threshold is below the Current Limit threshold. The Overcurrent Detection Shutdown Control Timer is initiated at the Overcurrent Shutdown Threshold which starts before the Current Limit is reached.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Overcurrent Shutdown (BIT13 = 1)

Effected outputs will turn off when the Overcurrent Shutdown Threshold has been breached for the Overcurrent Shutdown Delay Time. The respective OLD status bit will be set to a “1” and the driver will latch off. The driver can only be turned back on via the SPI port with a SPI command that includes an SRR = 1.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

OVERCURRENT DETECTION SHUT DOWN

OCD Input Bit 13	OUTx OCD Condition	Output Data Bit 13 Over Load Detect (OLD) Status	OUTx Status	Current Limit of all Drivers
0	0	0	Unchanged	3 A (typ.)
0	1	1 (Need SRR to reset)	OUTx Latches off after 200 μs (typ.) (Need SRR to reset)	3 A (typ.)
1	0	0	Unchanged	3 A (typ.)
1	1	1 (Need SRR to reset)	OUTx Latches Off After 25 μs (typ.) (Need SRR to reset)	3 A (typ.)

Overcurrent Detection Shut Down Control Timer

There are two protection mechanisms for output current, overcurrent and current limit.

1. Current limit − Always active with a typical threshold of 3 A.
2. Overcurrent Detection − Selectable shutdown time via Bit 13 with a typical threshold of 1.45 A.

Figure 6 shows the typical performance of a part which has exceeded the 1.45 A Overcurrent Detection threshold and started the shutdown control timer. When Bit 13 = 1, the shutdown time is 25 μsec. When Bit 13 = 0, the shutdown time is 200 μsec.

Once an Overcurrent Shutdown Delay Time event has been detected by the NCV7708F, the timer setting cannot be interrupted by an attempted change via a SPI command of Bit 13.

Input Bit 13	Overcurrent Shutdown Delay Time
0	200 μsec
1	25 μsec

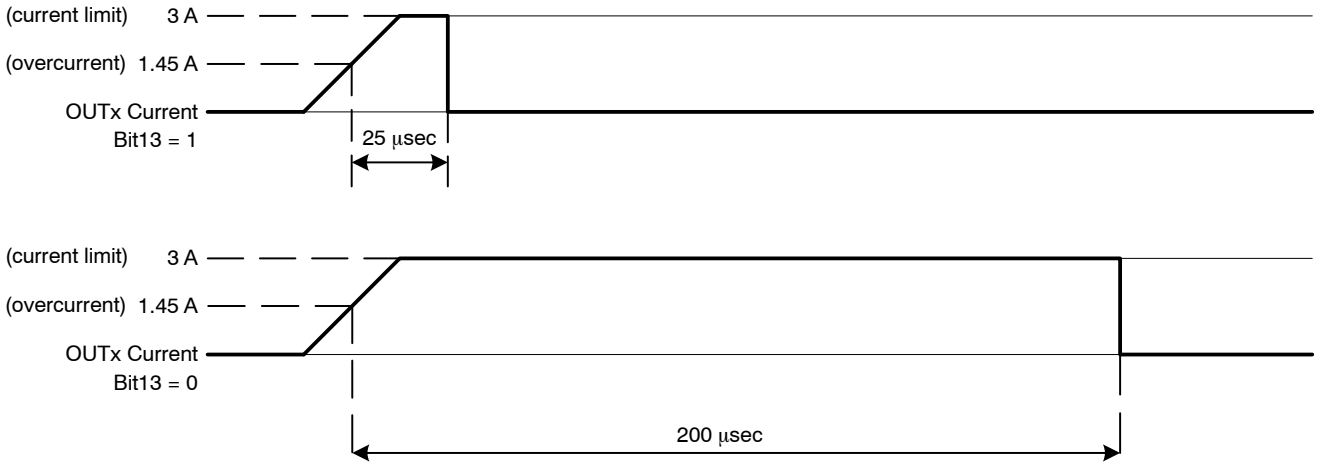


Figure 6. Output Current Shutdown Control

Under Load Detection

The under−load detection is accomplished by monitoring the current from each output driver. A minimum load current (this is the maximum detection threshold) is required when the drivers are turned on. If the under−load circuit detection threshold has been crossed for more than the under−load delay time, the bit indicator (output bit #14) will be set to a 1. In addition, the offending driver will be turned off only if input bit 14 (ULD) is set to 1 (true).

The NCV7708F uses a global under load timer. An under load condition starts the global under load delay timer. If under load occurs in another channel after the global timer has been started, the delay for any subsequent under load will be the remainder of the initially started timer. The timer runs continuously with any persistent under load condition. The under load detect bit is reset by setting input data bit 0, SRR = 1.

UNDER LOAD DETECTION SHUT DOWN

ULD Input Bit 14	OUTx ULD Condition	Output Data Bit 14 Under Load Detect (ULD) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	OUTx Latches Off (Need SRR to reset)

Undervoltage Lockout (PSF)

Undervoltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins. When the Undervoltage Threshold level has been breached on both or either one of the VSx supply inputs, output bit 15 (PSF) will be set and all outputs will turn off.

Turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re−established, the programmed outputs will return to programmed operation.

The Power Supply Fail bit is reset by setting input data bit 0, SRR = 1.

UNDERVOLTAGE LOCK OUT (UVLO) SHUT DOWN

VSx UVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status
0	0	Unchanged
1	1 (Need SRR to reset)	All Outputs Off (Remain off until VSx is out of UVLO)

Overvoltage Shutdown (PSF)

Overvoltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins. When the Overvoltage Threshold voltage level has been breached on both or either one of the VSx supply inputs, output bit 15 will be set and, if input bit 15 (OVLO) is set to 1, all drivers will turn off. Turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re−established, the programmed outputs will turn back on. Overvoltage shutdown can be disabled by using the SPI input bit 15 (OVLO = 0). The Power Supply Fail bit is reset by setting input data bit 0, SRR = 1.

OVERVOLTAGE LOCK OUT (OVLO) SHUT DOWN

OVLO Input Bit 15	VSx OVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	All Outputs Latch Off while in OVLO Return to programmed state out of OVLO

Thermal Shutdown

Six independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two levels, one to give a Thermal Warning (TW) and a higher one, Thermal Shutdown, which will shut the drivers off. When the part reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set to a 1, and the outputs will remain on. With one or more sensors detecting the thermal shutdown level, all channels will be turned off simultaneously. All outputs will return to normal operation when the part thermally recovers (Thermal toggling), because the thermal shutdown does not change the channel selection. The output data bit 0, Thermal Warning, will latch and remain set, even after cooling, and is reset by using a software command to input bit 0 (SRR = 1). Since thermal warning precedes a thermal shutdown, software polling of this bit will allow for load control and possible prevention of thermal shutdown conditions.

Thermal warning information can be retrieved immediately without performing a complete SPI access cycle. Figure 7 displays how this is accomplished. Bringing the CSB pin from a 1 to a 0 with SI = 0 immediately displays the information on output data bit 0, thermal warning. As the temperature of the NCV7708F changes from a condition from below the thermal warning threshold to above the thermal warning threshold, the state of the SO pin changes and this level is available immediately when the CSB goes to 0. A 0 on SO indicates there is no thermal warning, while a 1 indicates the IC is above the thermal warning threshold. This warning bit is reset by setting input data bit 0, SRR = 1.

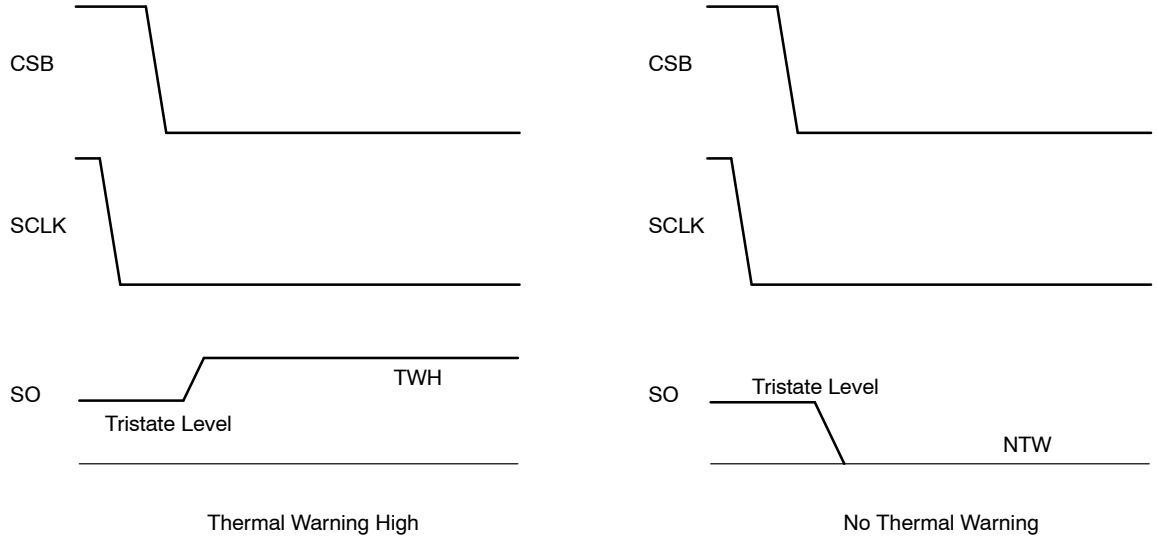


Figure 7. Access to Temperature warning information shows the thermal information is available immediately with activation of the CSB signal without having to toggle the SCLK line.

Applications Drawing

The applications drawing below displays the range with which this part can drive a multitude of loads.

1. H−Bridge Driver configuration
2. Low Side Driver
3. High Side Driver

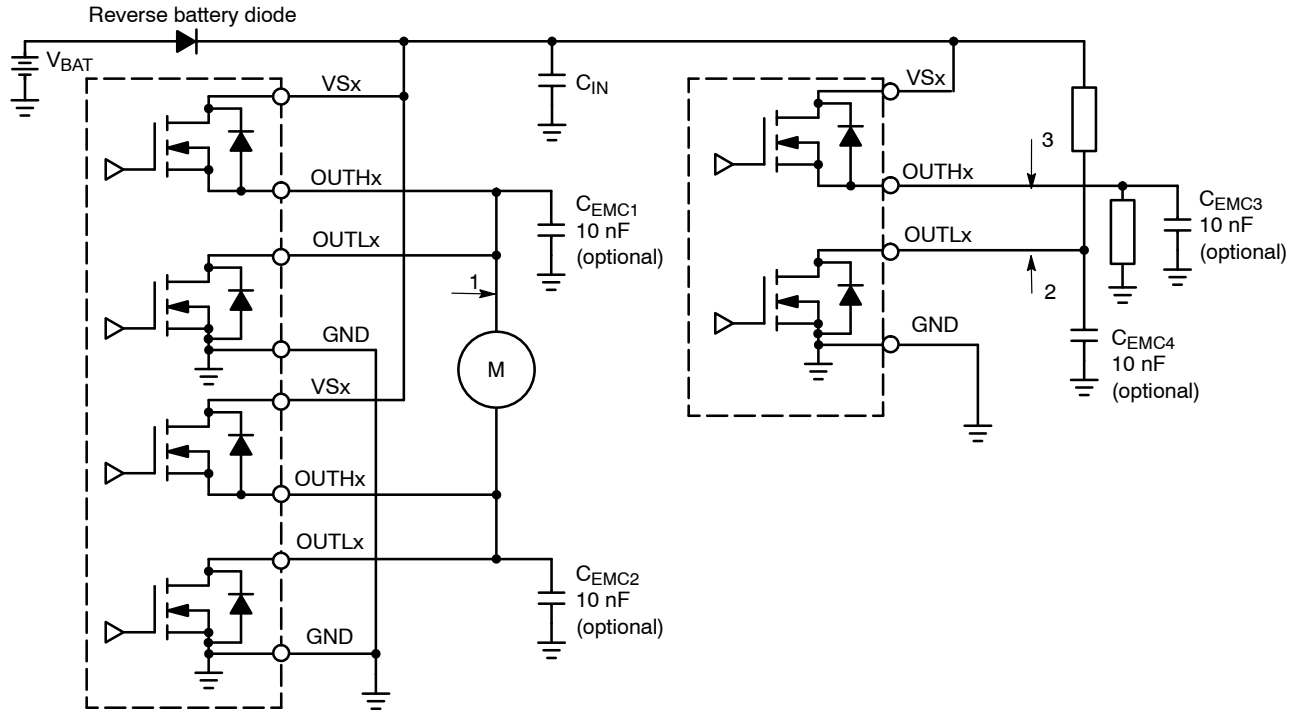


Figure 8. Application Drawing

Any combination of H−Bridge, high−side, or low−side drivers can be designed in. This allows for flexibility in many systems.

H−Bridge Driver Configuration

The NCV7708F has the flexibility of controlling each driver independently. When the device is set up in an H−Bridge configuration, the software design has to take care of avoiding simultaneous activation of connected HS and LS transistors. Resulting high shoot through currents could cause irreversible damage to the device.

Overvoltage Clamping − Driving Inductive Loads

To avoid excessive voltages when driving inductive loads in a single−side−mode (LS or HS switch, no freewheeling path), the NCV7708F provides internal clamping diodes. Thus any load type can be driven without the requirement of external freewheeling diodes. Due to high power dissipation during clamping, the maximum energy capability of the driver transistor has to be considered.

TYPICAL OPERATING CHARACTERISTICS

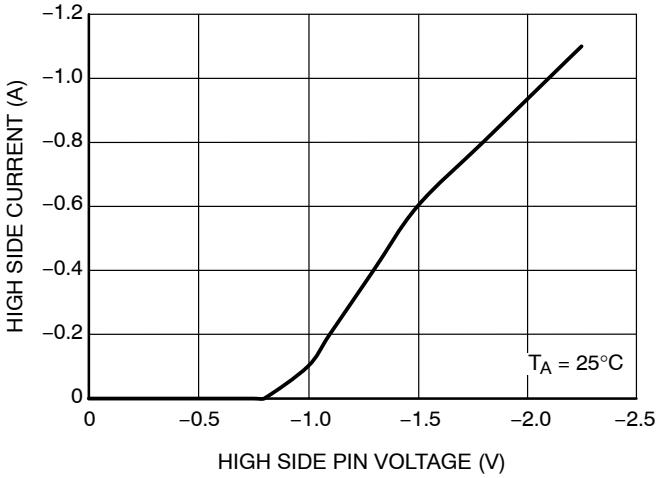


Figure 9. High−Side Negative Clamp Voltage vs. Reverse Current

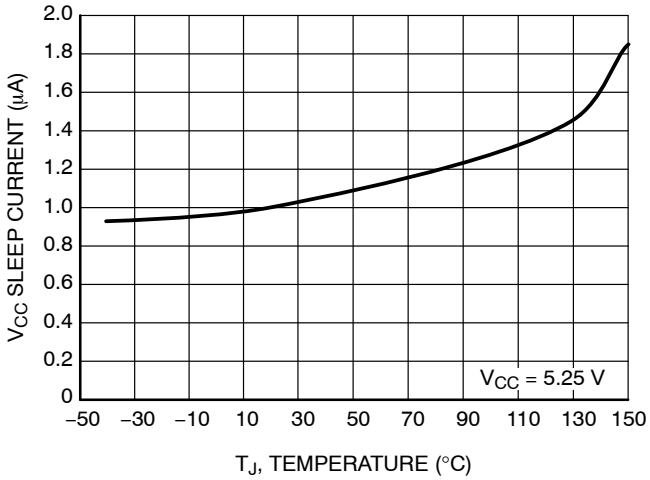


Figure 10. V_{CC} Sleep Supply Current vs. Temperature

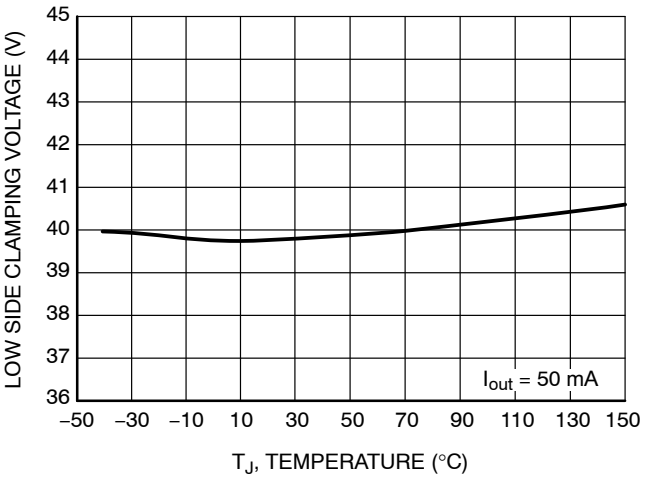


Figure 11. Low−Side Clamping Voltage vs. Temperature

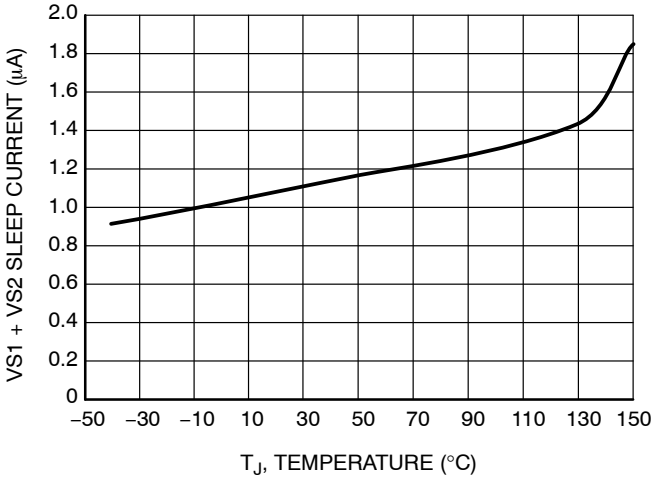


Figure 12. VS1 + VS2 Sleep Current vs. Temperature

Table 1. FAULT HANDLING

Fault	Fault Memory Serial Output Bit	Driver Condition During Fault	Driver Condition after Parameters Within Specified Limits	Output Register Clear Requirement
Current Limit ± 3 A (Input OCD Bit 13 = 0)*	Latched	Offending Driver is latched off after 200 μsec	Offending Driver is latched off	Valid SPI frame with SRR set to 1
Over Load ± 1.45 A (Input OCD Bit 13 = 1)*	Latched	Offending Driver is latched off by overcurrent timer after 25 μsec	Offending Driver is latched off	Valid SPI frame with SRR set to 1
Under Load (Input ULD Bit 14 = 0)	Latched	Unchanged	Unchanged	Valid SPI frame with SRR set to 1
Under Load (Input ULD Bit 14 = 1)	Latched	Offending Driver is latched off after 350 μsec	Offending Driver is latched off	Valid SPI frame with SRR set to 1 falls below
Power Supply Fail (OVLO)	Latched	Output Driver on	Bit 15 = 0 Outputs return to their previous programmed state	PSF bit is cleared when VSx falls below the hysteresis voltage level and SRR set to 1
		Output Driver switched to high Z	Bit 15 = 1 Outputs return to their previous programmed state	PSF bit is cleared when VSx falls below the hysteresis voltage level and SRR set to 1
Power Supply Fail (UVLO)	Latched	Output Driver switched to high Z	Return to programmed state	Valid SPI frame with SRR set to 1
Thermal Warning (TW)	Latched	Output Driver on	Drivers in Normal Operation	Valid SPI frame with SRR set to 1
Thermal Shutdown	No Thermal Shutdown Bit	All Drivers turns off	Return to programmed state	No Thermal Shutdown Bit

All specified currents and times refer to typical numbers.
*Current Limit performance is independent of Overcurrent (Bit13). The output will always limit to current limit independent of bit 13.

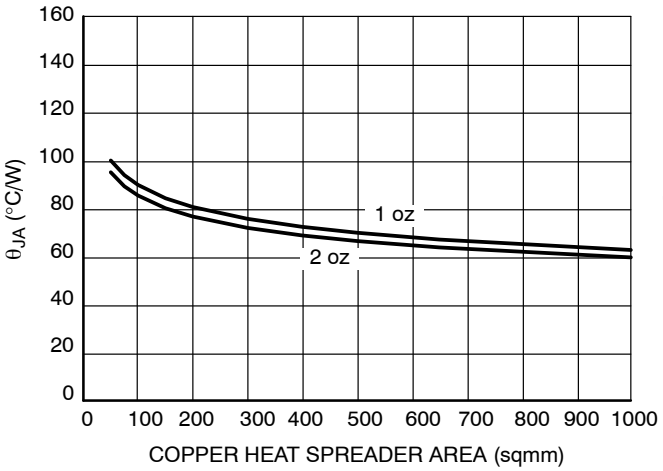


Figure 13. SOIC−28 θ_{JA} vs. Copper Spreader Area

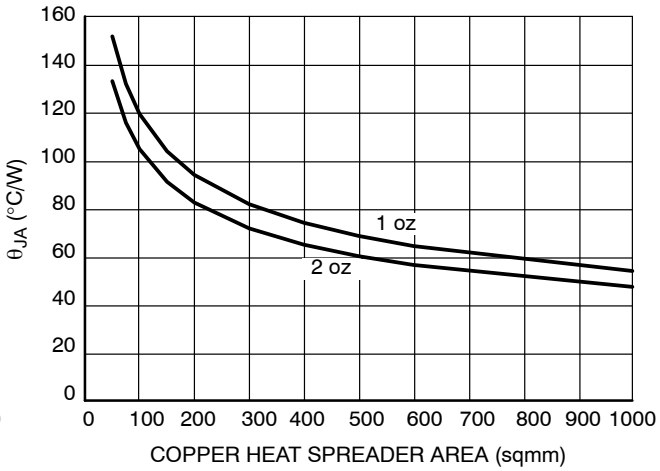


Figure 14. SSOP24 Narrow Body Exposed Pad θ_{JA} vs. Copper Spreader Area

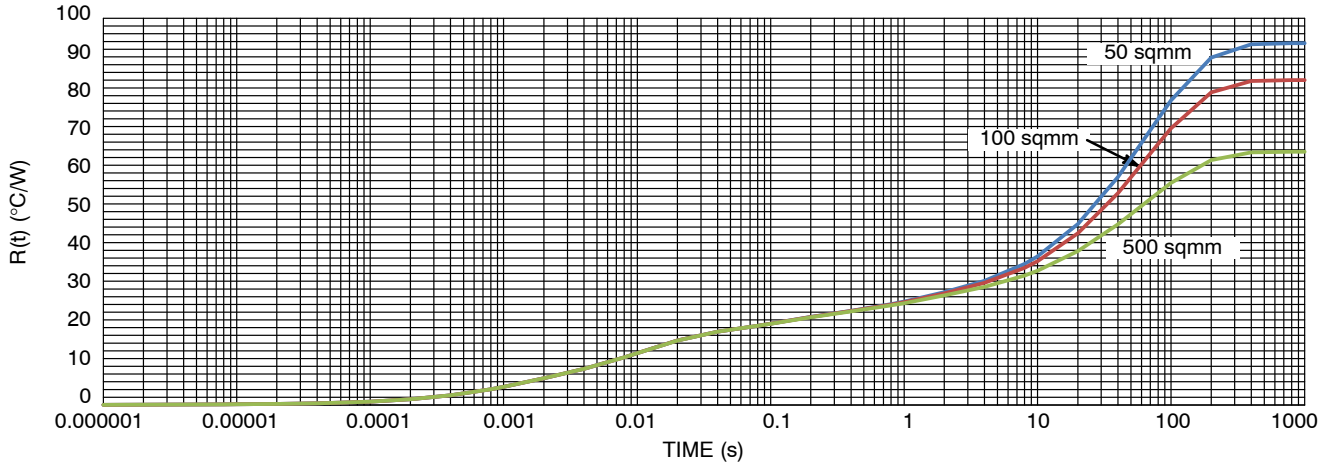


Figure 15. SOIC 28−Lead Single Pulse Heating Curve

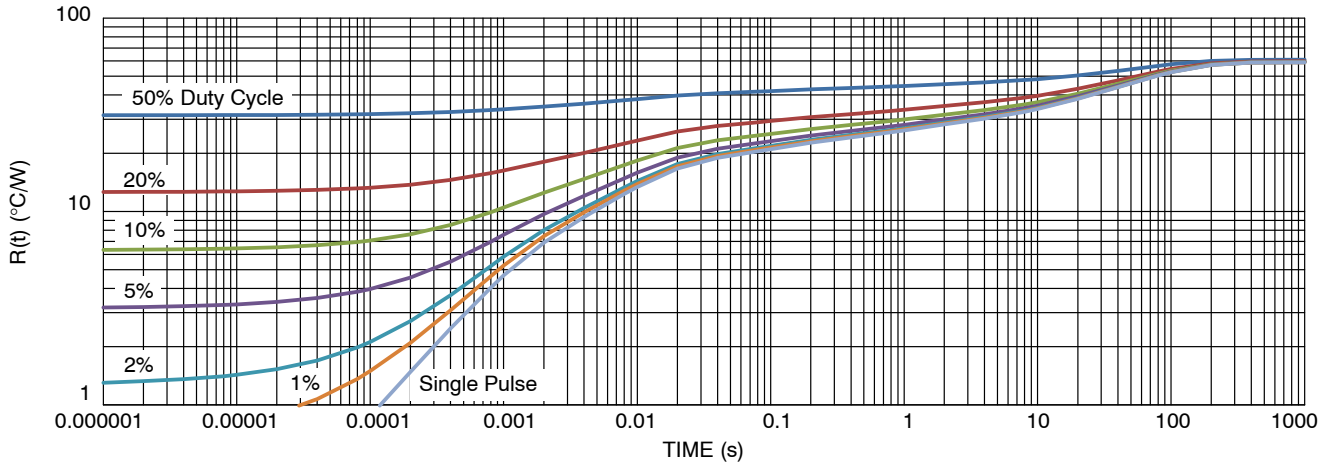


Figure 16. SOIC 28−Lead Thermal Duty Cycle Curve on 986 mm^2 Spreader Test Board

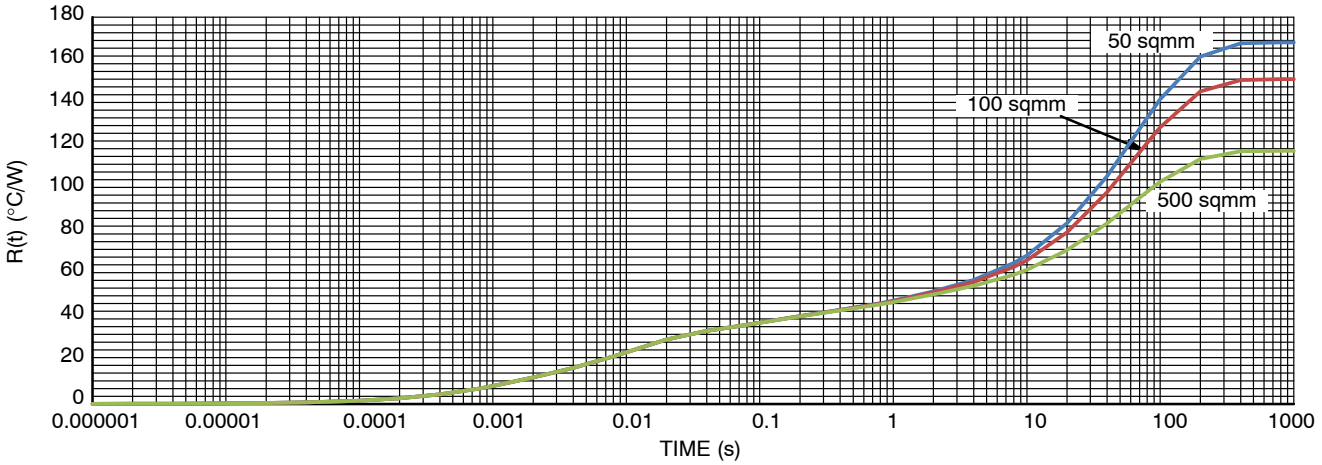


Figure 17. SSOP24 Narrow Body Exposed Pad Single Pulse Heating Curve

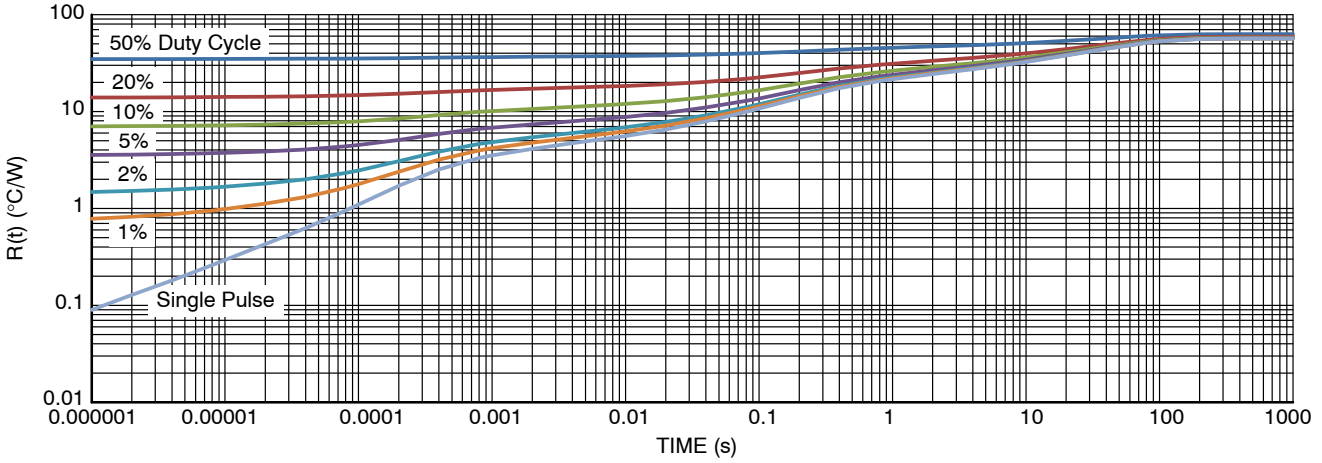
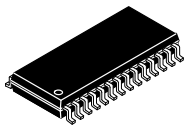


Figure 18. SSOP24 Lead Single Pulse Heating Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

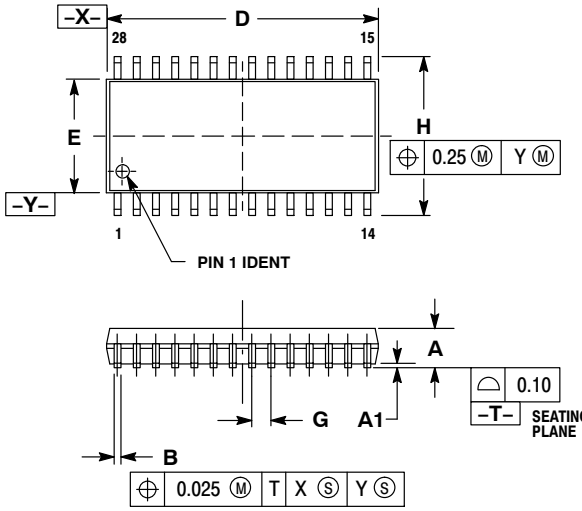
ON Semiconductor®

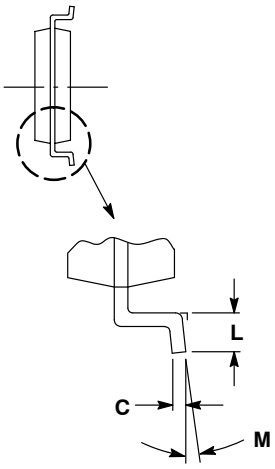


SCALE 1:1

SOIC−28 WB
CASE 751F
ISSUE J

DATE 23 SEP 2015

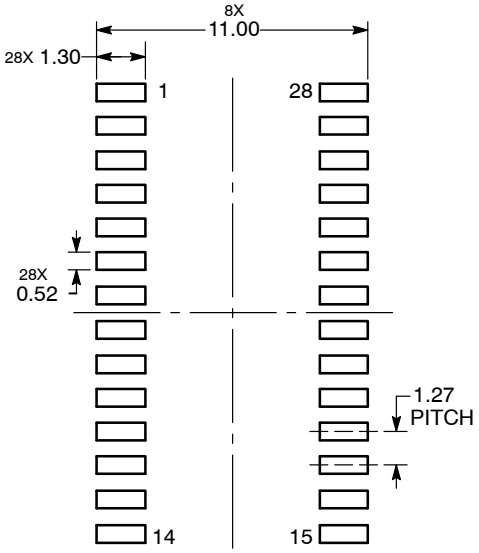




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

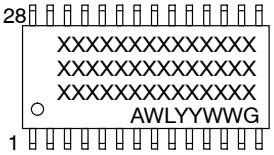
	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**SOIC−28 WIDE BODY**	**PAGE 1 OF 1**

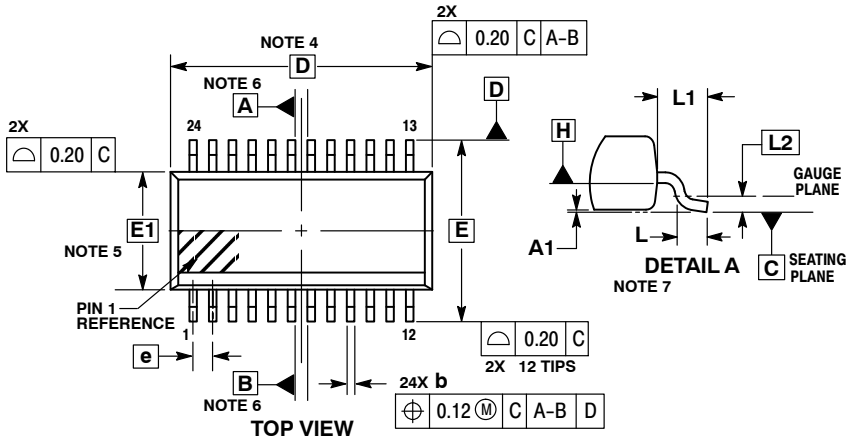
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

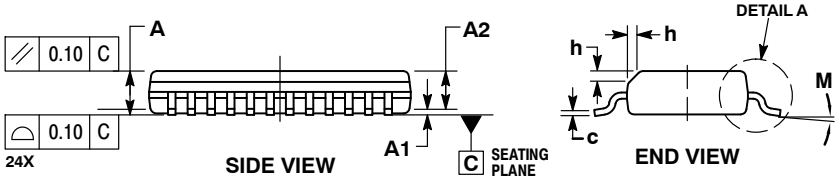
ON Semiconductor®

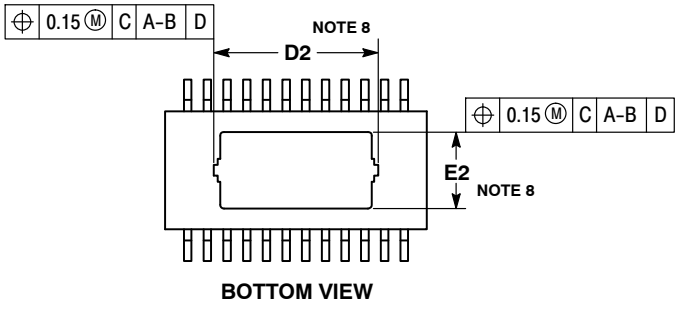
SCALE 1:1

SSOP24 NB EP
CASE 940AK
ISSUE O

DATE 24 APR 2012



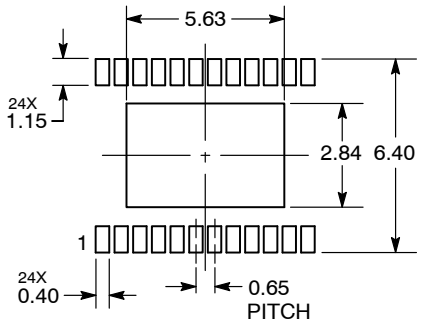




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

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(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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