

# Silicon Carbide (SiC) MOSFET - EliteSiC, 56 mohm, 650 V, M2, TOLL NTBL075N065SC1

## Features

- Typ.  $R_{DS(on)} = 56 \text{ m}\Omega @ V_{GS} = 18 \text{ V}$   
Typ.  $R_{DS(on)} = 75 \text{ m}\Omega @ V_{GS} = 15 \text{ V}$
- Ultra Low Gate Charge ( $Q_{G(tot)} = 59 \text{ nC}$ )
- Low Effective Output Capacitance ( $C_{oss} = 109 \text{ pF}$ )
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- RoHS Compliant

## Typical Applications

- SMPS (Switching Mode Power Supplies)
- Solar Inverters
- UPS (Uninterruptable Power Supplies)
- Energy Storage

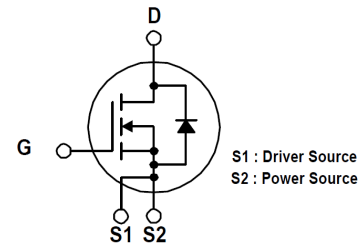
## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	650	V
Gate-to-Source Voltage		$V_{GS}$	-8/+22.6	V
Recommended Operation Values of Gate - Source Voltage		$T_C < 175^\circ\text{C}$	$V_{GSop}$	-5/+18 V
Continuous Drain Current (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	37 A
			$P_D$	139 W
Power Dissipation (Note 2)	Steady State	$T_C = 100^\circ\text{C}$	$I_D$	26 A
			$P_D$	69 W
Pulsed Drain Current (Note 3)		$T_C = 25^\circ\text{C}$	$I_{DM}$	101 A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	37	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 12.9 \text{ A}_{pk}$ , $L = 1 \text{ mH}$ ) (Note 4)		$E_{AS}$	83	mJ
Maximum Lead Temperature for Soldering (1/8" from Case for 5 Seconds)		$T_L$	260	$^\circ\text{C}$

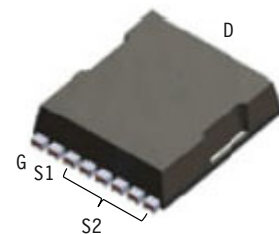
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in 2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4.  $E_{AS}$  of 83 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1 \text{ mH}$ ,  $I_{AS} = 12.9 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $V_{GS} = 18 \text{ V}$ .

$V_{DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
650 V	85 m $\Omega @ 18 \text{ V}$	37 A

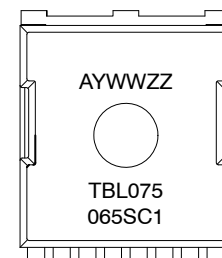


N-Channel MOSFET



H-PSOF8L  
CASE 100DC

## MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- TBL075065SC1 = Specific Device Code

## ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NTBL075N065SC1

## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	1.08	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	43	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 20\text{ mA}$ , refer to $25^\circ\text{C}$ (Note 5)		0.12		V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 650\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$ (Note 5)		1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +18/-5\text{ V}, V_{DS} = 0\text{ V}$			250	nA

## ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 5\text{ mA}$	1.8	2.8	4.3	V
Recommended Gate Voltage	$V_{GOP}$		-5		+18	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 15\text{ A}, T_J = 25^\circ\text{C}$		75		m $\Omega$
		$V_{GS} = 18\text{ V}, I_D = 15\text{ A}, T_J = 25^\circ\text{C}$		56	85	
		$V_{GS} = 18\text{ V}, I_D = 15\text{ A}, T_J = 175^\circ\text{C}$ (Note 5)		70		
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$ (Note 5)		8		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz},$ $V_{DS} = 325\text{ V}$ (Note 5)		1191		pF
Output Capacitance	$C_{OSS}$			109		
Reverse Transfer Capacitance	$C_{RSS}$			11		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 520\text{ V},$ $I_D = 15\text{ A}$ (Note 5)		59		nC
Gate-to-Source Charge	$Q_{GS}$			17		
Gate-to-Drain Charge	$Q_{GD}$			20		
Gate-Resistance	$R_G$	$f = 1\text{ MHz}$		5.6		$\Omega$

## SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 400\text{ V},$ $I_D = 15\text{ A}, R_G = 2.2\ \Omega,$ Inductive Load (Note 5)		9		ns
Rise Time	$t_r$			12		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	$t_f$			8		$\mu\text{J}$
Turn-On Switching Loss	$E_{ON}$			35		
Turn-Off Switching Loss	$E_{OFF}$			12		
Total Switching Loss	$E_{TOT}$			47		

## SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Source-Drain Diode Forward Current	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$ (Note 5)			37	A
Pulsed Source-Drain Diode Forward Current (Note 3)	$I_{SDM}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$ (Note 5)			101	A
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 15\text{ A}, T_J = 25^\circ\text{C}$		4.4		V

# NTBL075N065SC1

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### SOURCE-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = -5/18 V, I <sub>SD</sub> = 15 A, dI <sub>S</sub> /dt = 1000 A/μs (Note 5)		16		ns
Reverse Recovery Charge	Q <sub>RR</sub>		66		nC	
Reverse Recovery Energy	E <sub>REC</sub>		2.6		μJ	
Peak Reverse Recovery Current	I <sub>RRM</sub>		8.4		A	
Charge time	T <sub>a</sub>		8.6		ns	
Discharge time	T <sub>b</sub>		7.1		ns	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

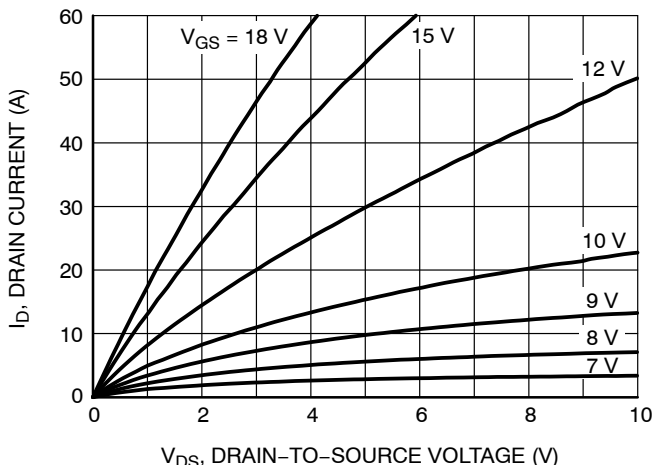


Figure 1. On-Region Characteristics

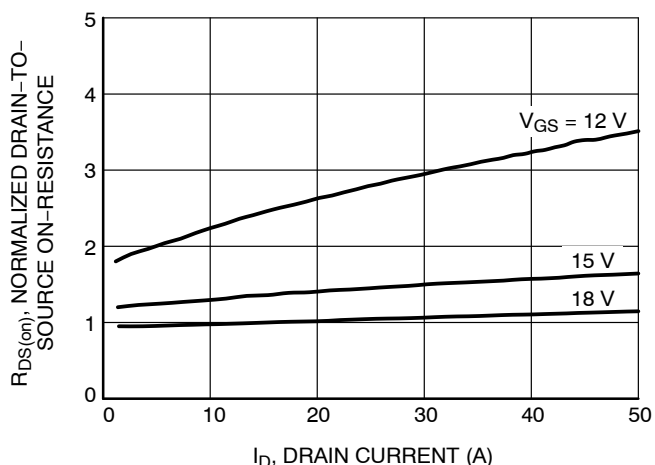


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

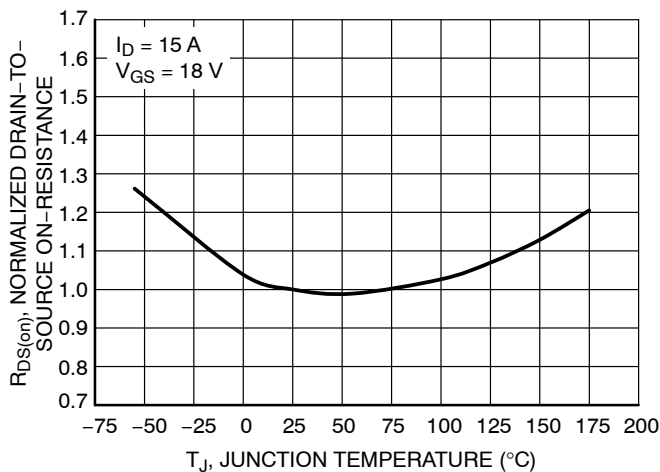


Figure 3. On-Resistance Variation with Temperature

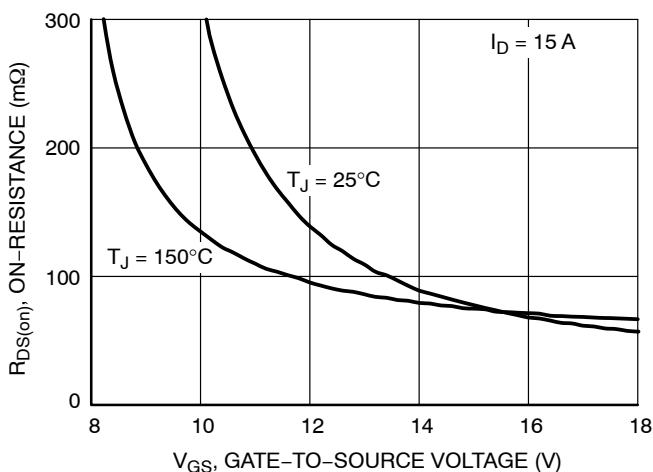


Figure 4. On-Resistance vs. Gate-to-Source Voltage

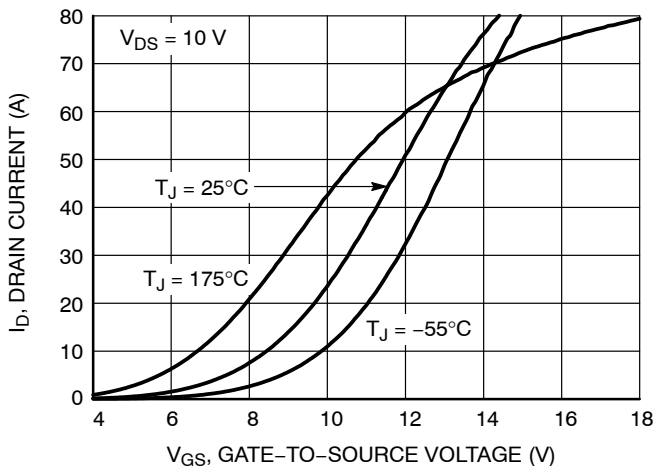


Figure 5. Transfer Characteristics

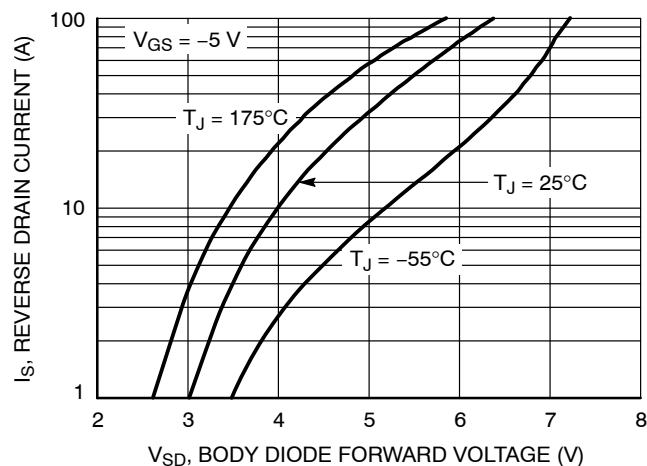


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

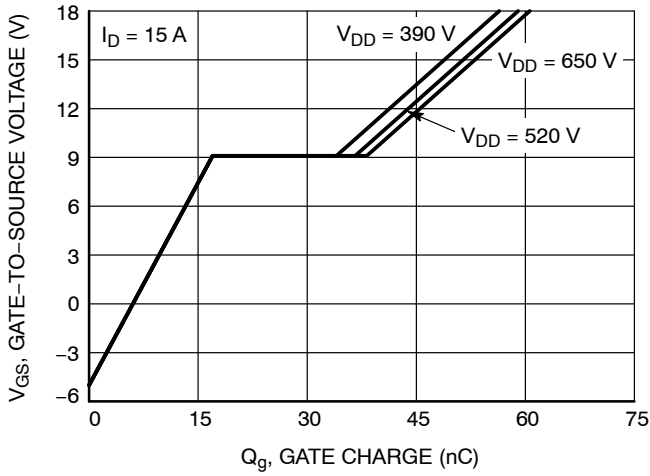


Figure 7. Gate-to-Source Voltage vs. Total Charge

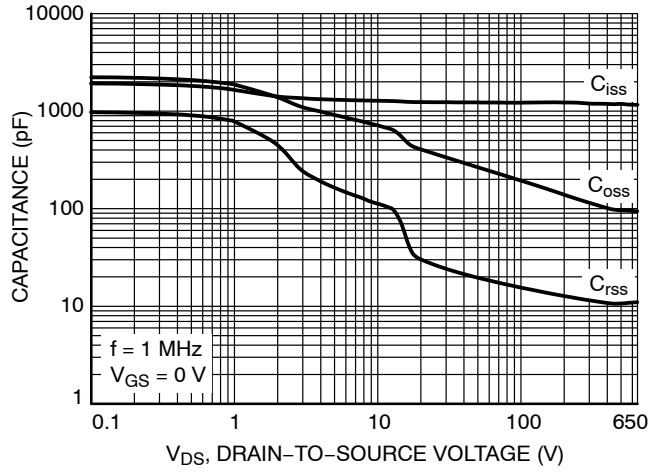


Figure 8. Capacitance vs. Drain-to-Source Voltage

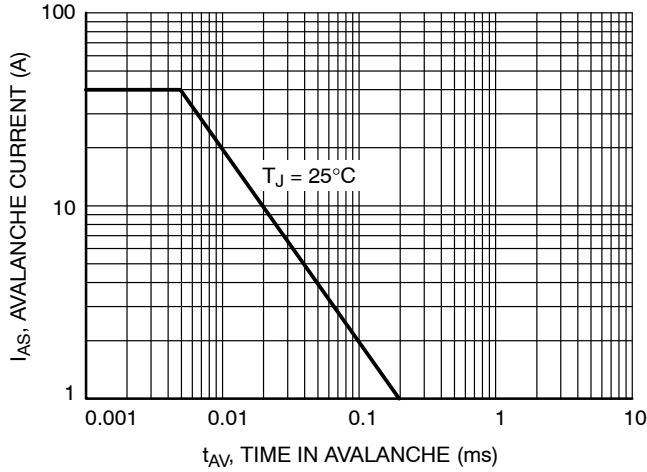


Figure 9. Unclamped Inductive Switching Capability

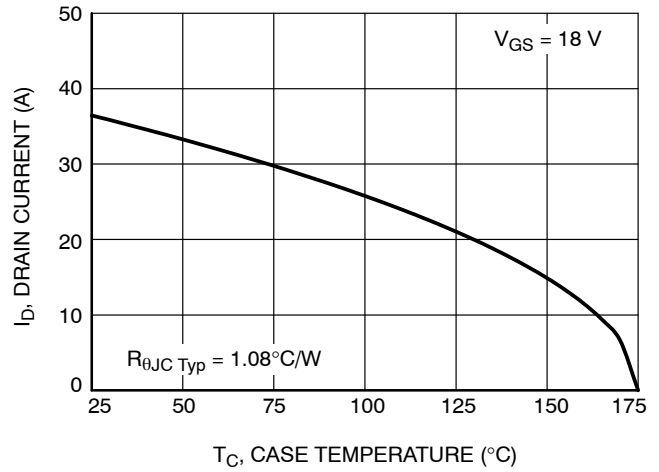


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

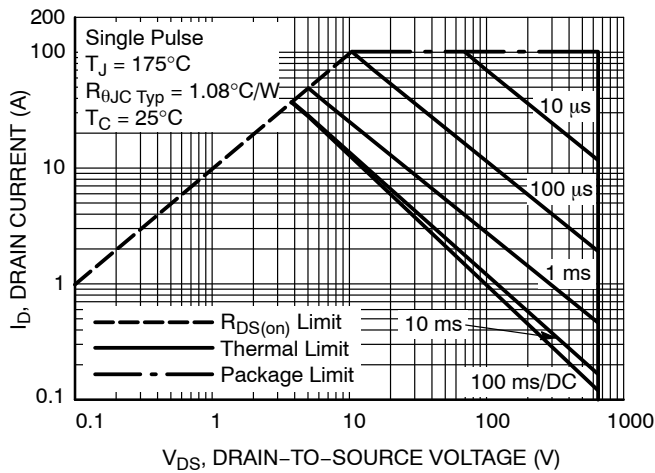


Figure 11. Safe Operating Area

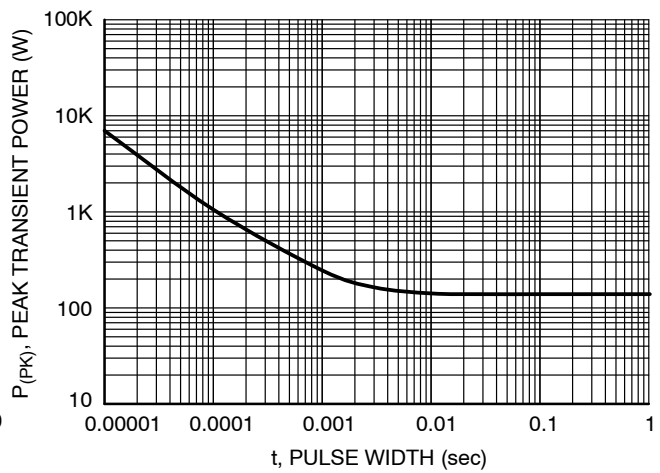


Figure 12. Single Pulse Maximum Power Dissipation

# NTBL075N065SC1

## TYPICAL CHARACTERISTICS

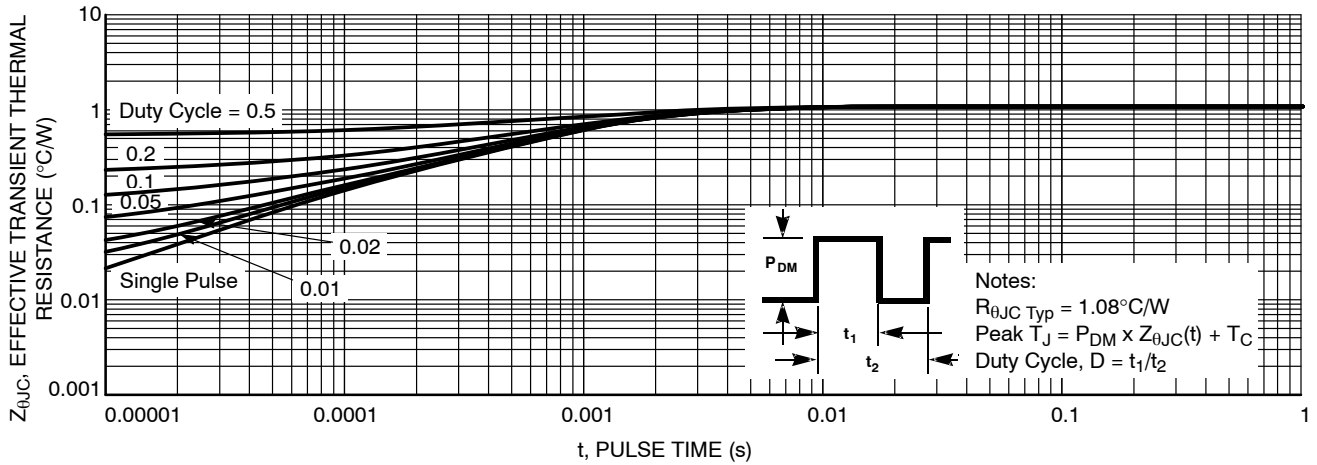


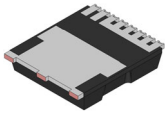
Figure 13. Junction-to-Case Transient Thermal Response

### DEVICE ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBL075N065SC1	H-PSOF8L	2000 / Tape & Reel

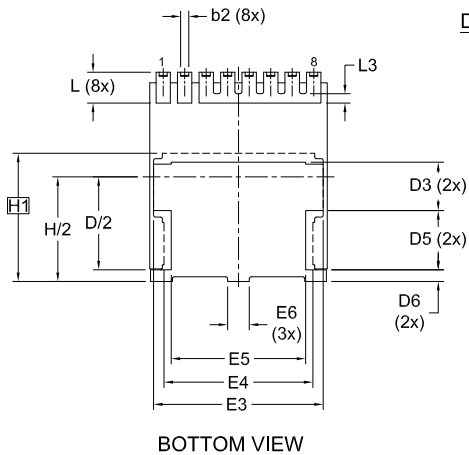
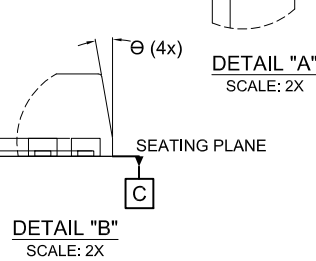
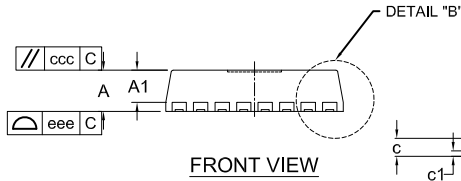
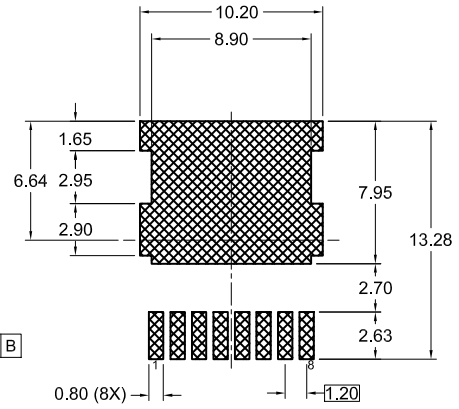
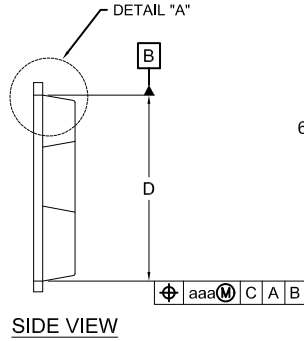
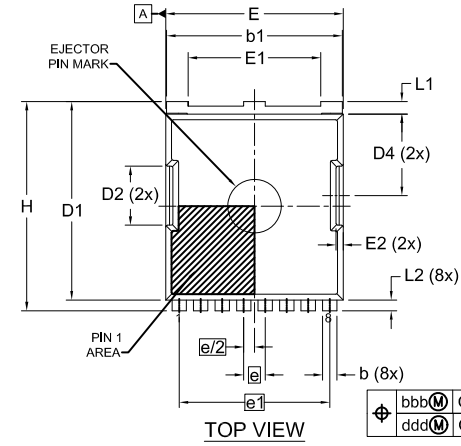
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

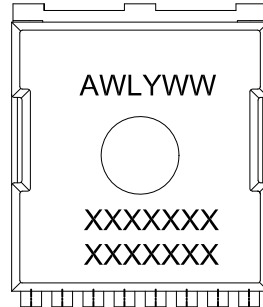


**H-PSOF8L 9.90x11.68, 1.20P**  
CASE 100DC  
ISSUE A

DATE 18 MAY 2023



### GENERIC MARKING DIAGRAM\*



A = ASSY LOCATION  
WL = WAFER LOT CODE  
Y = YEAR CODE  
WW = WORK WEEK CODE  
XXXXXXXX = DEVICE CODE  
XXXXXXXX = DEVICE CODE

\*THIS INFORMATION IS GENERIC.  
PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  3. CONTROLLING DIMENSION: MILLIMETERS.
  4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
  5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	---	---
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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