Electrical Rules Check Report

Class	Document	Message
		Successful Compile for GazeT_IR_LED.PrjPcb

Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\Projects\GAZET_IR_LED_DRIVER\design_f

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=2.438mm) (Preferred=0.203mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=3.048mm) (All)	0
Hole To Hole Clearance (Gap=0.203mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.102mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.046mm) (InComponent('C9') And HasPad('C9-pos')),(InComponent('C10') And	0
Minimum Solder Mask Sliver (Gap=0.046mm) (InComponent('C11') And HasPad('C11-pos')),(InComponent('C12') And	0
Minimum Solder Mask Sliver (Gap=0.076mm)	0
Silk To Solder Mask (Clearance=0.076mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.102mm) (All),(All)	0
Silk to Silk (Clearance=0.097mm) (InComponent('R4') And IsText),(OnLayer('Bottom Overlay'))	0
Silk to Silk (Clearance=0.061mm) (InComponent('TP2') And IsArc And OnLayer('Bottom Overlay')),(OnLayer('Bottom	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=40.64mm) (Prefered=12.7mm) (All)	0
Total	0