

Notes:

- ① Material: UL recognized component DE104i UL File Number: E41625, relative permittivity 4.37 nominal
- ② Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer $1 \div 4 \mu\text{m}$, gold layer $0.076 \div 0.2 \mu\text{m}$
- ③ All gerber files generated as a top view
4. Fabricate according IPC-A-600
 5. Non-conductive epoxy ink recommended for silkscreen
 6. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
 7. All holes diameter refer to final diameter after eventual plating
 8. Solder mask tenting is applied on number of vias both on top layer

Gerber file extensions table

Gerber files	
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	Top layer L1_TOP
.GBL	Bottom layer L2_BOTTOM
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Bottom side silkscreen
.GM1	Board outline

Drill file extensions table

Drill files	
.TXT	Layer pair L1_TOP to L2_BOTTOM

STR-DMS-CONTROL-GEVB*PCB fabrication notes and requirements*

Engineer: T. Duris

Date: 12. May 2021 18:03

PCB File: GazeT_CONTROL_BOARD.PcbDoc

Repository revision: Not in repository control

Revision:
rev0.1**State:**
releasedFabrication
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A

A

Layer Stack

Material	Layer	Thickness	Dielectric Material	Permittivity	Type	Gerber
	Top Paste				Paste Mask	GTP
	Top Overlay				Legend	GTO
Surface Material	Top Solder	0.0150mm(0.591mil)	Solder Resist		Solder Mask	GTS
Copper	L1_TOP	0.0180mm(0.709mil)			Signal	GTL
Core		1.5000mm(59.055mil)	Isola DE104i	3.86	Dielectric	
Copper	L2_BOTTOM	0.0180mm(0.709mil)			Signal	GBL
Surface Material	Bottom Solder	0.0150mm(0.591mil)	Solder Resist		Solder Mask	GBS
	Bottom Overlay				Legend	GBO
	Bottom Paste				Paste Mask	GBP
Total thickness: 1.5660mm(61.655mil)						

B

B

C

C

D

D

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Layer stack details		Fabrication document	Sheet 2 / 12
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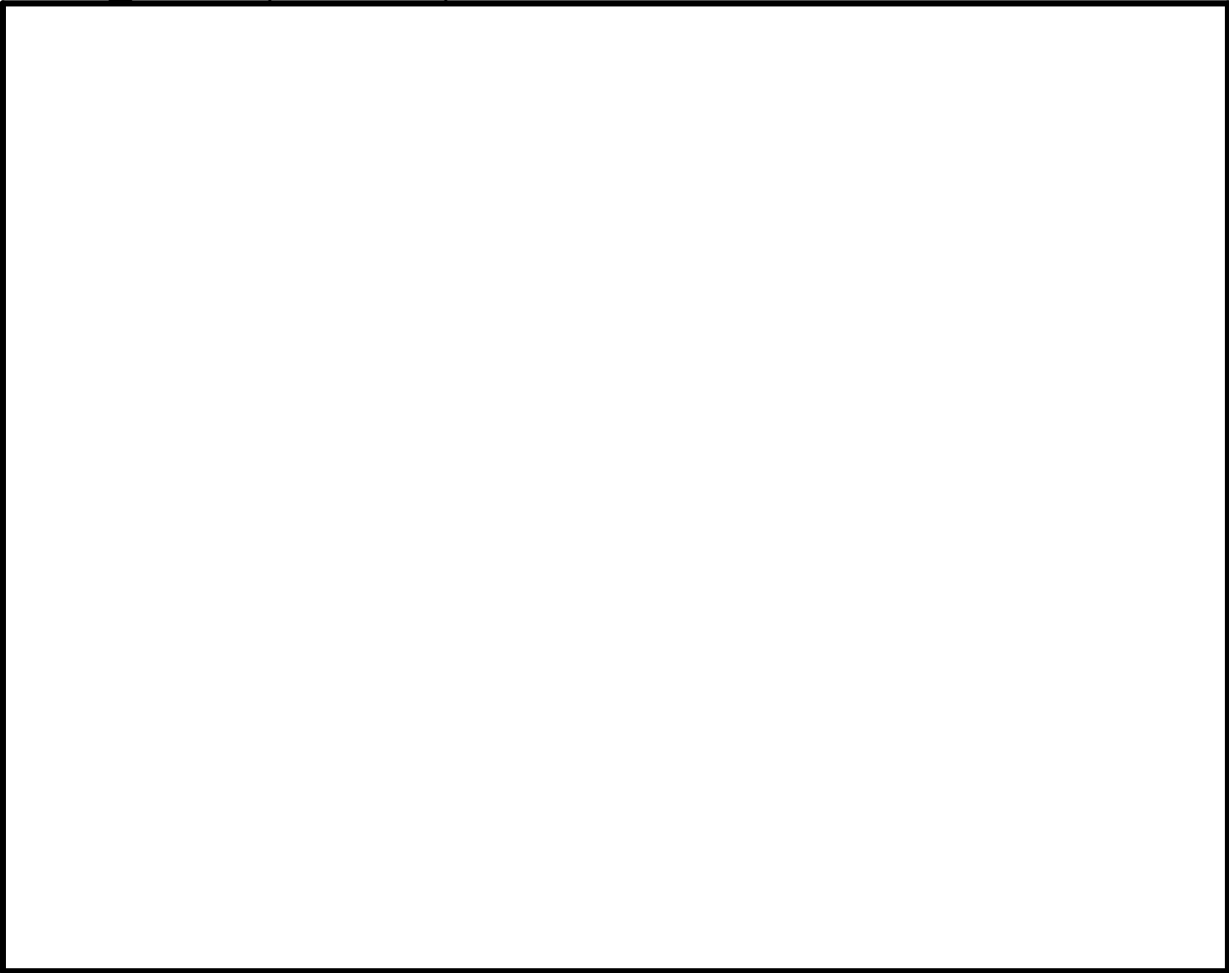
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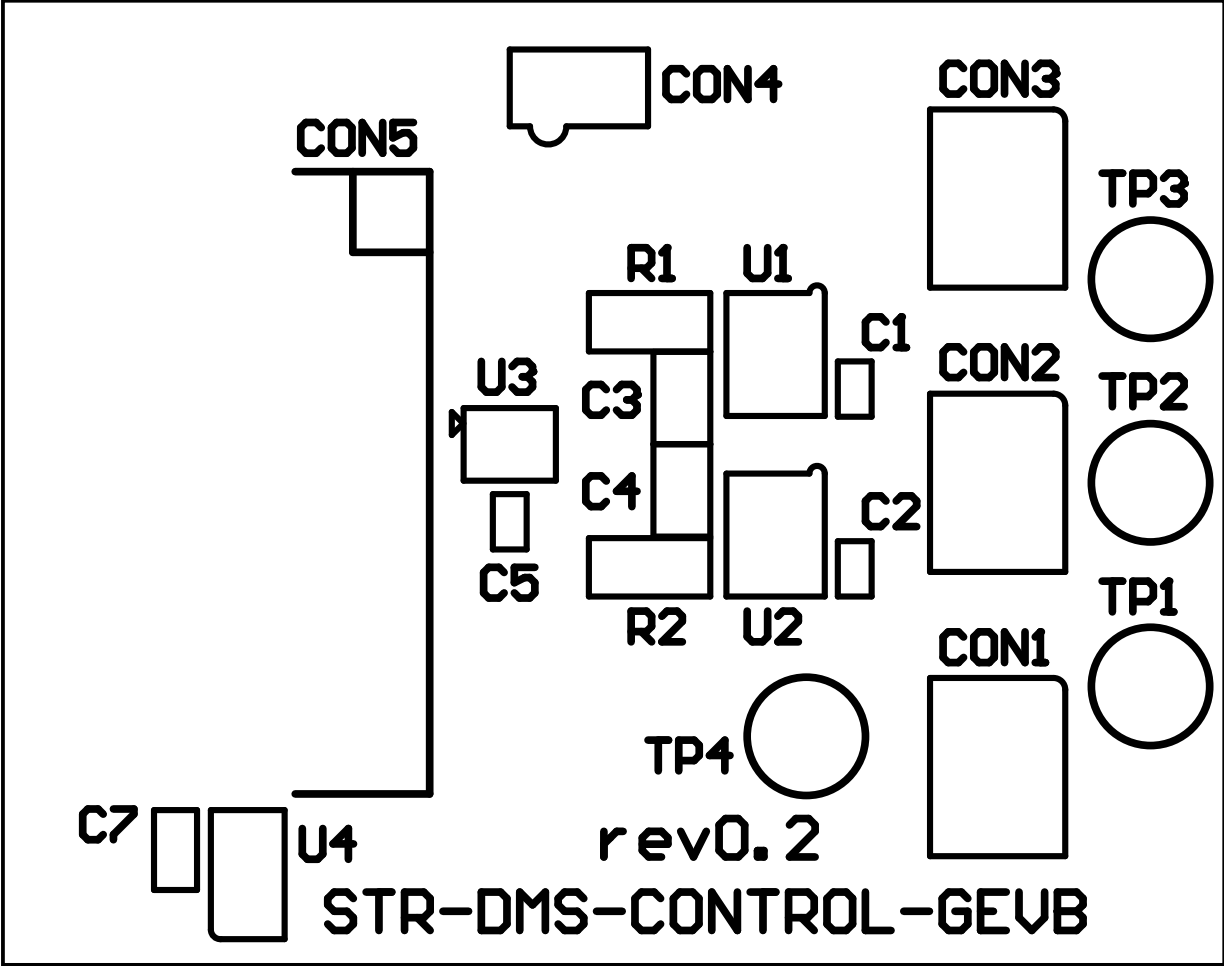
Board outline (Scale 4:1)



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<i>Board outline definition - top view 4:1</i>		Fabrication document	Sheet 3 / 12
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Top Overlay (Scale 4:1)



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Top side silkscreen		Fabrication document	Sheet 4 / 12
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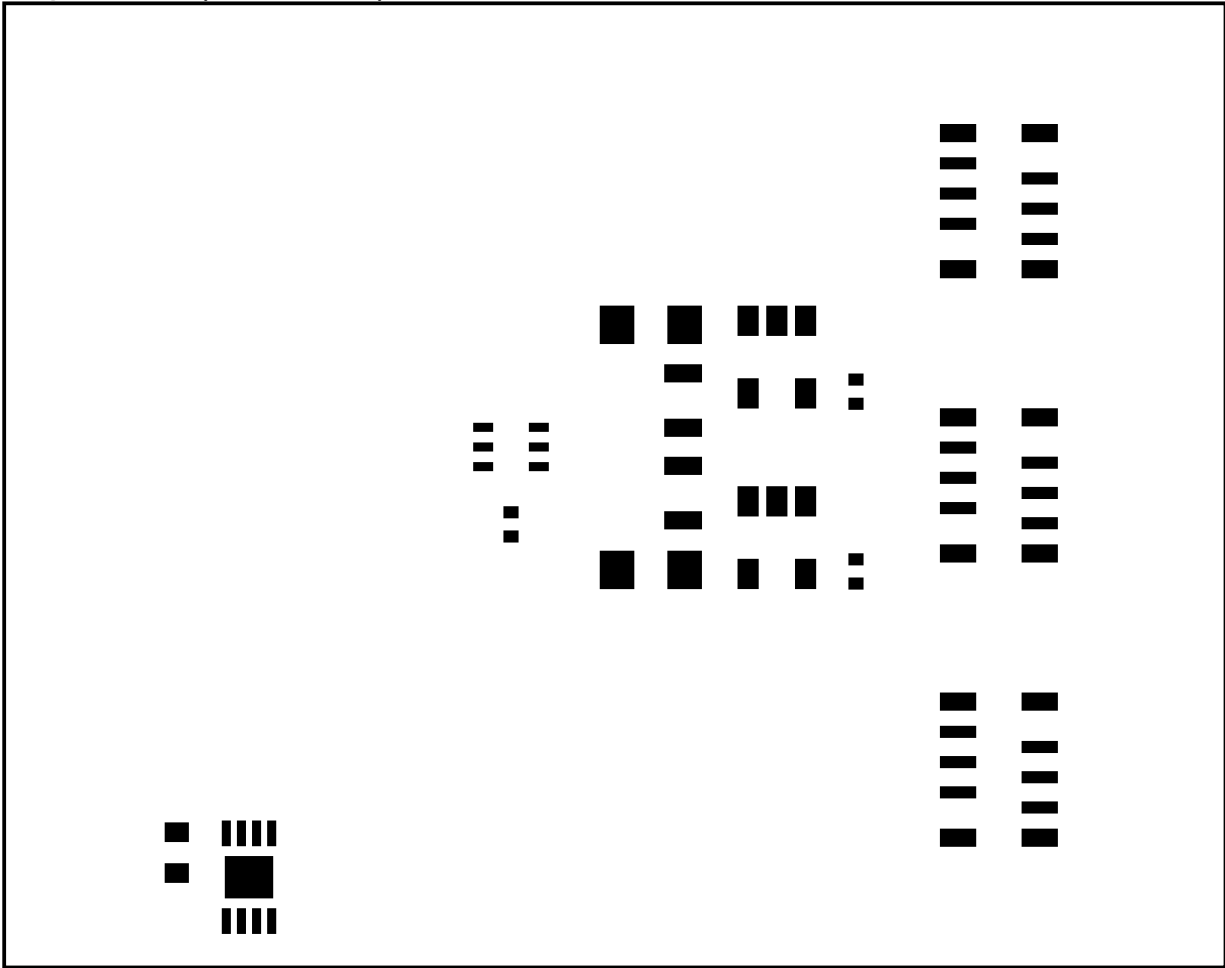
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Top Paste (Scale 4:1)



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<i>Top side solder paste</i>		Fabrication document	Sheet 5 / 12
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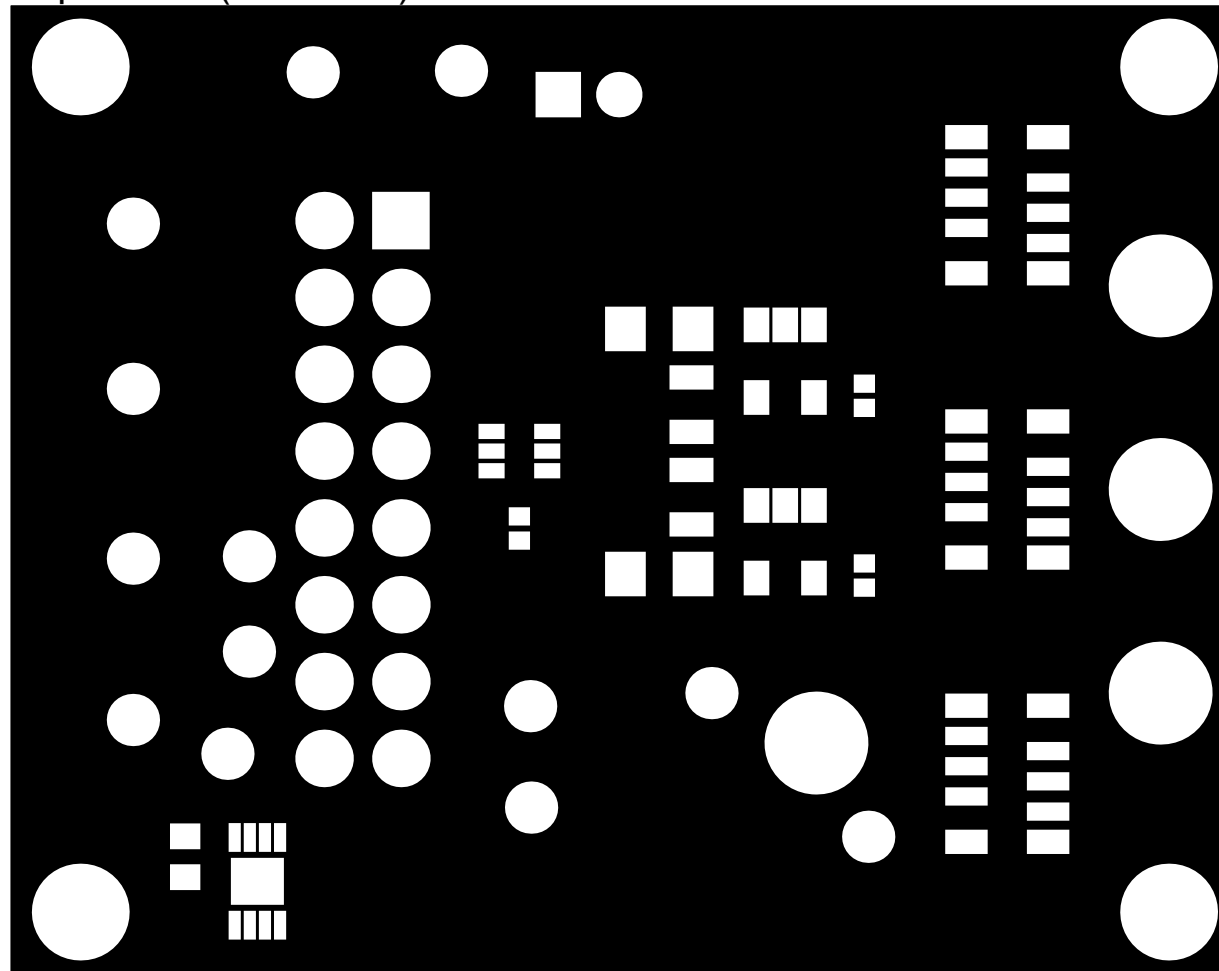
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Top Solder (Scale 4:1)



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Top side solder mask		Fabrication document	Sheet 6 / 12
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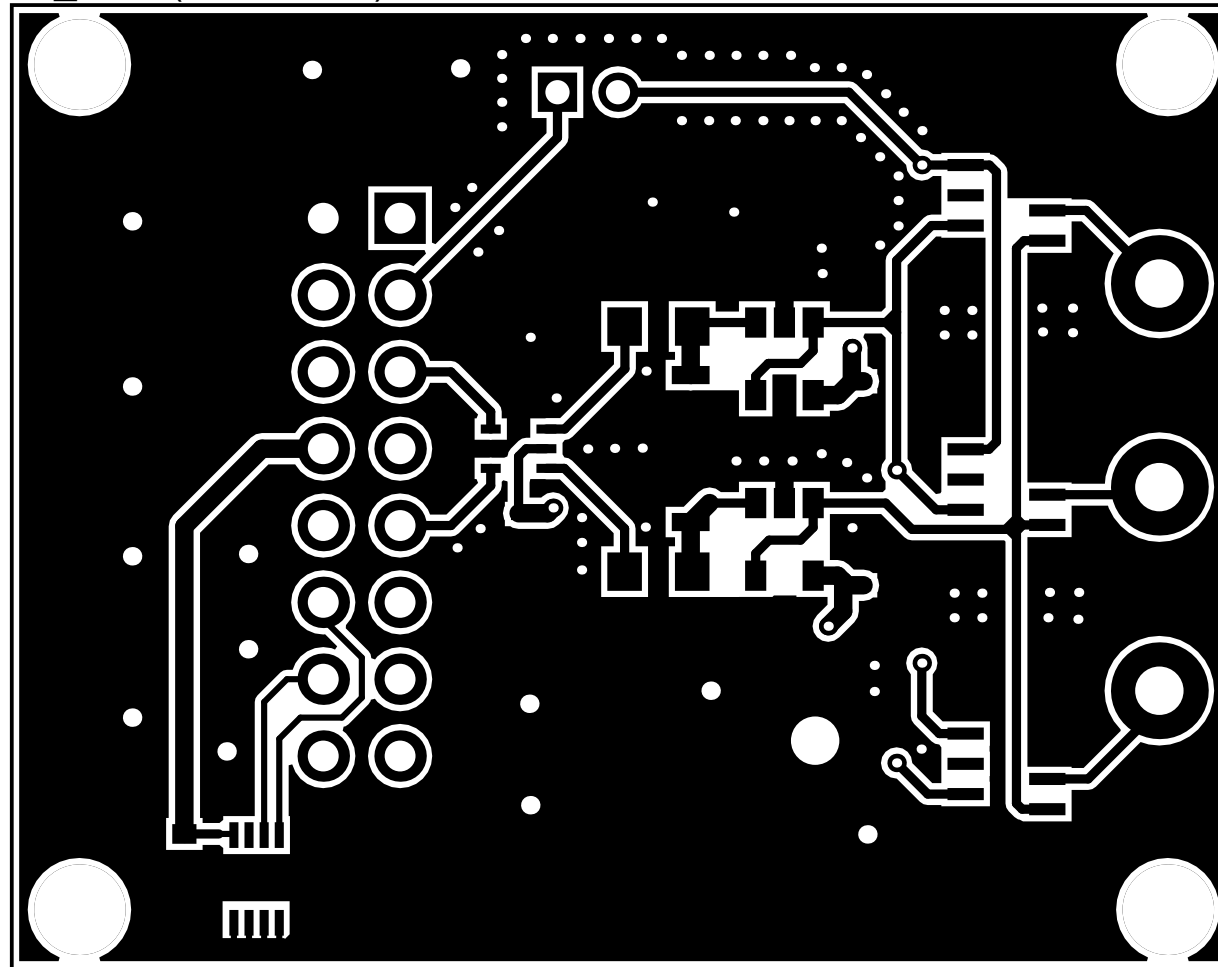
2


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4

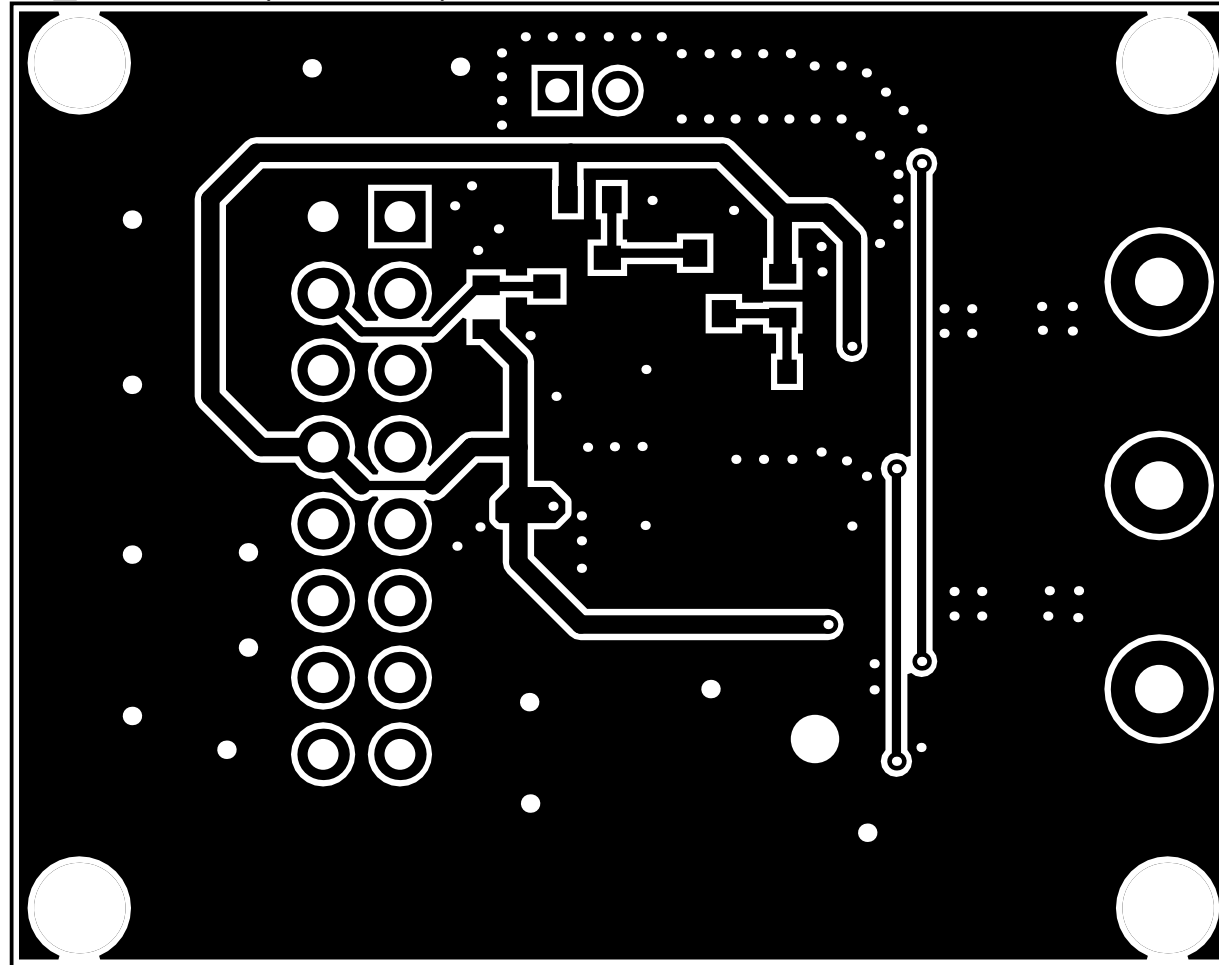
5

L1_TOP (Scale =4:1)



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Layer L1_TOP		Fabrication document	Sheet 7 / 12
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L2_BOTTOM (Scale 4:1)



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Layer L2_BOTTOM		Fabrication document	Sheet 8 / 12
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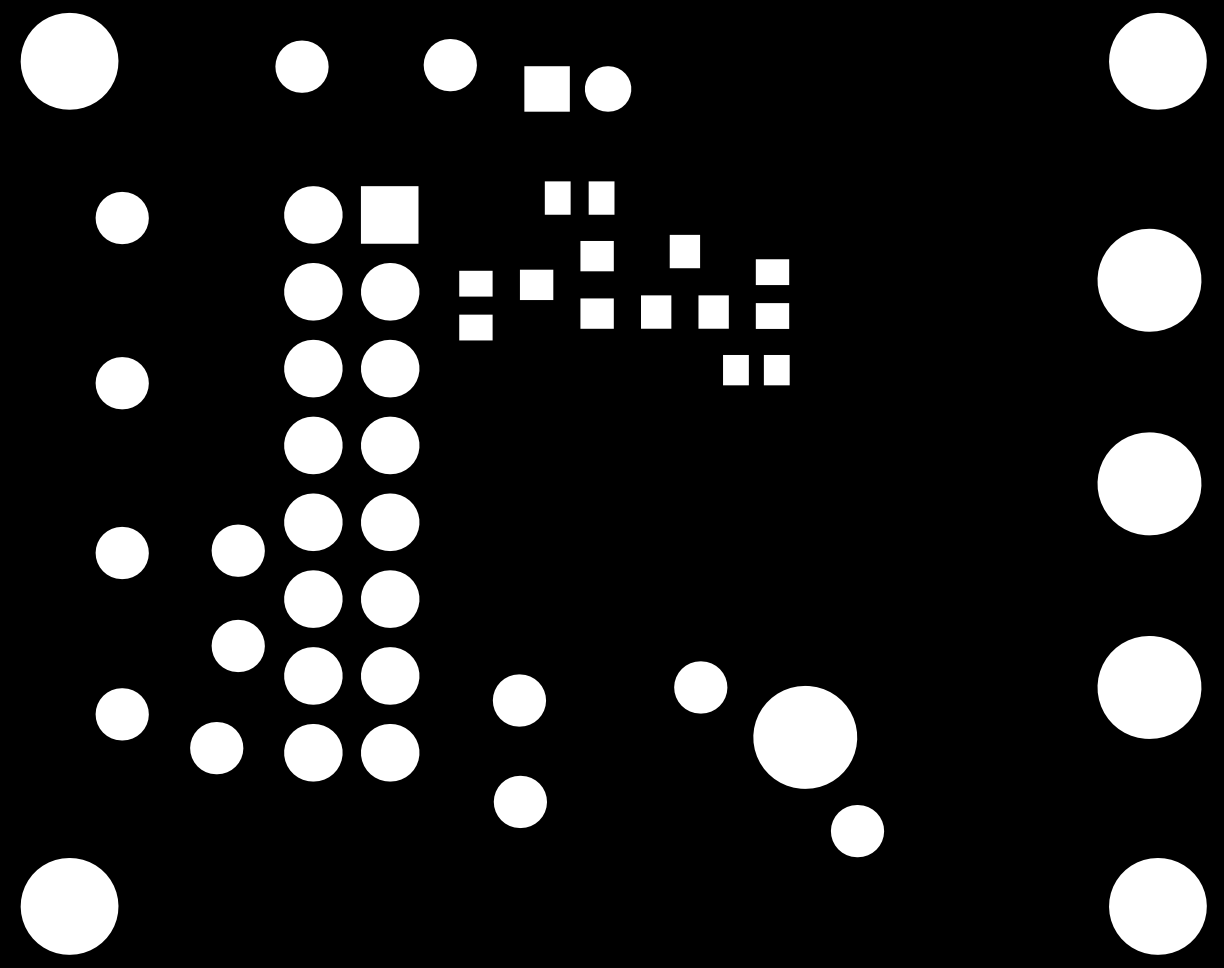
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Bottom Solder (Scale 4:1)



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Bottom side solder mask		Fabrication document	Sheet 9 / 12
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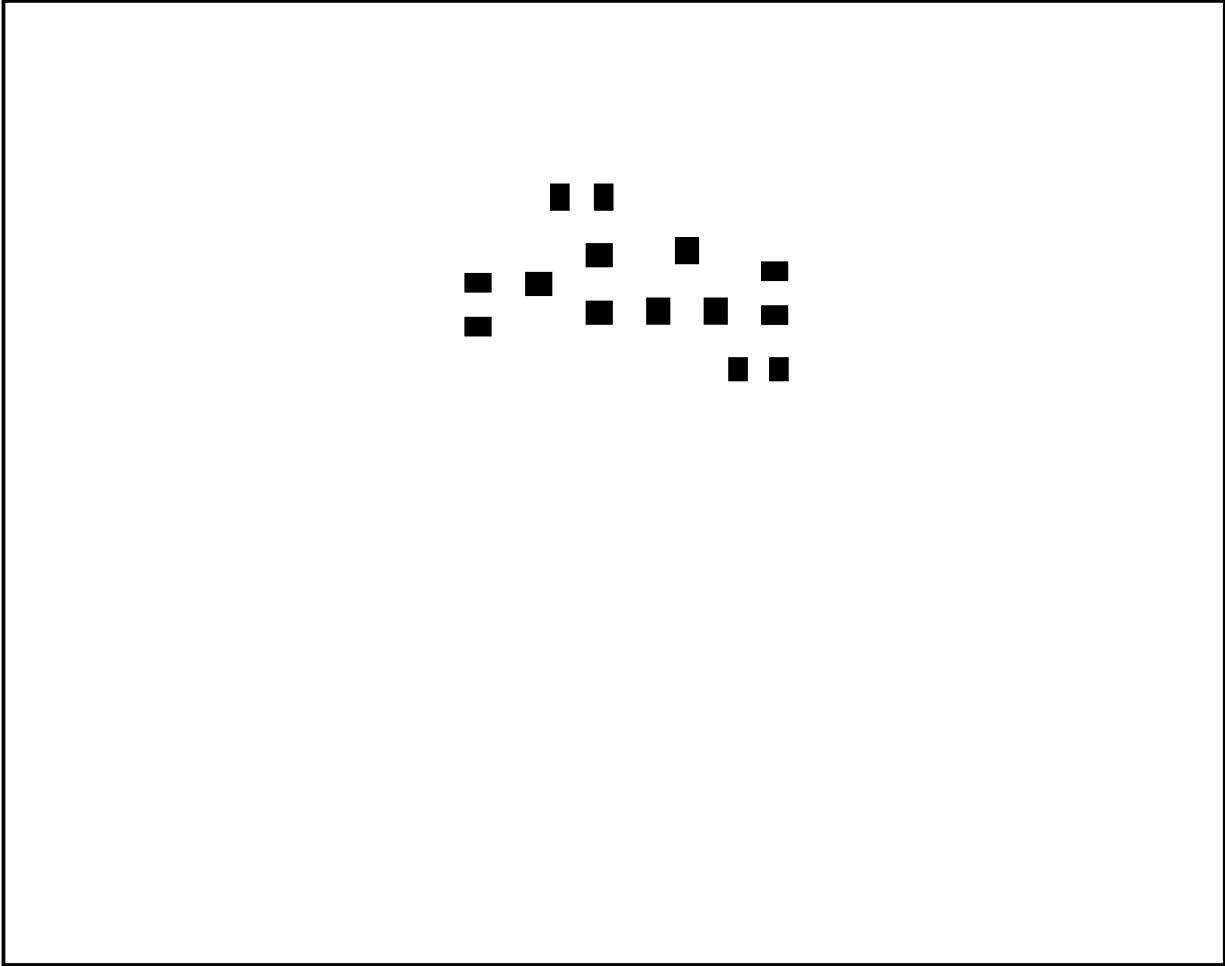
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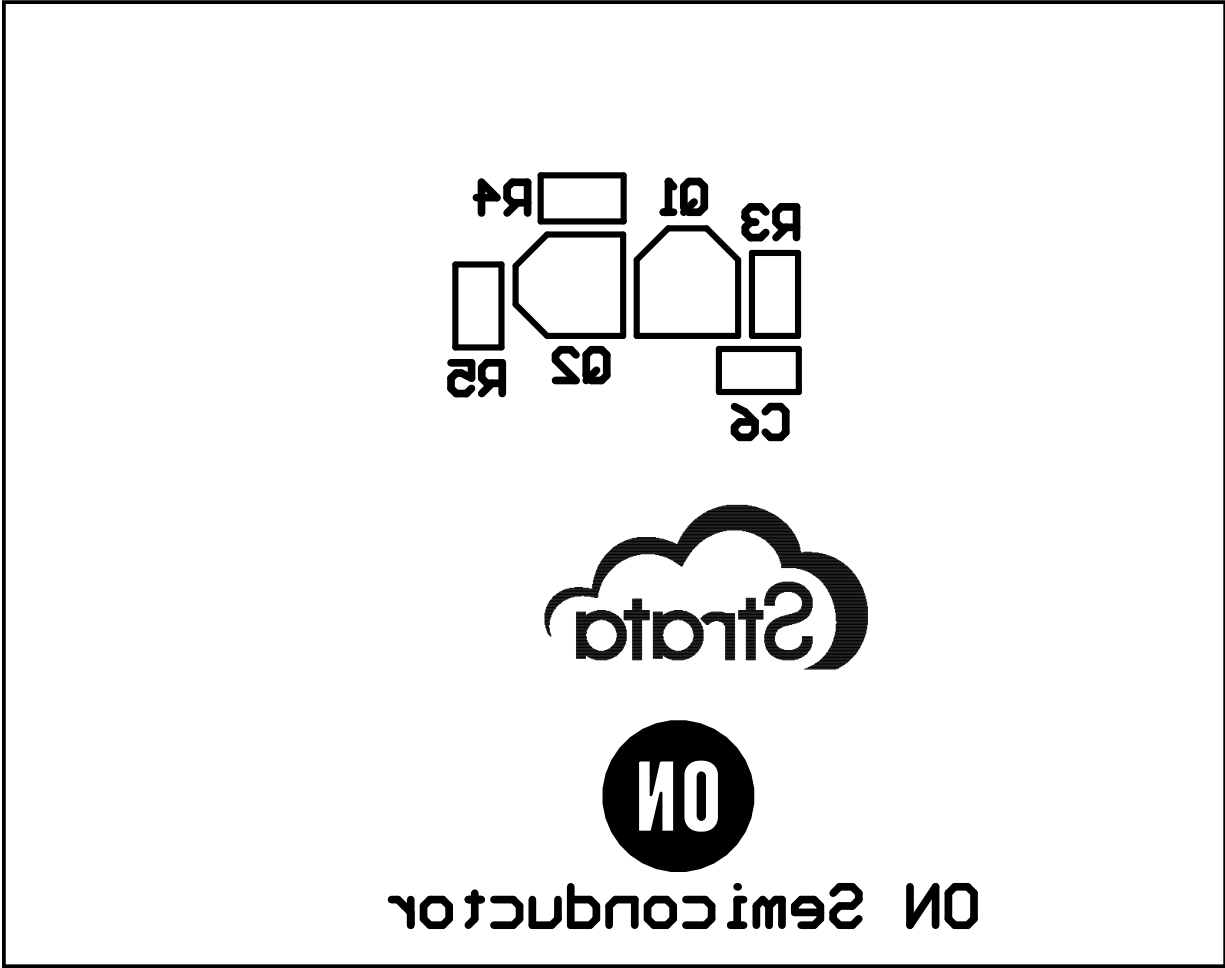
Bottom Paste (Scale 4:1)




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<i>Bottom side solder paste</i>		Fabrication document	Sheet 10 / 12
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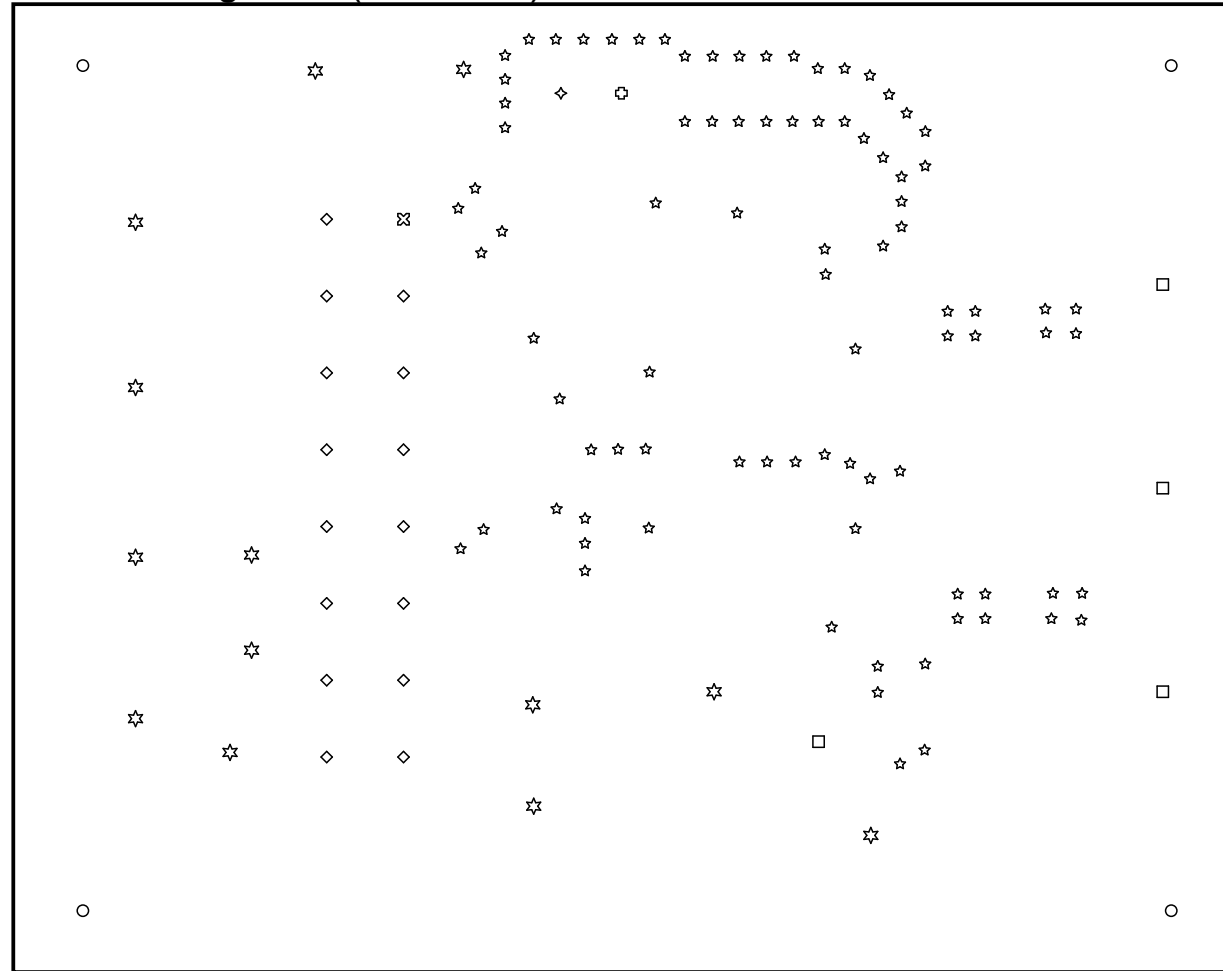
Bottom Overlay (Scale 4:1)



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Bottom side silkscreen		Fabrication document	Sheet 11 / 12
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Drill Drawing View (Scale 4:1)



Drill Table - vias

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
☆	87	0.305mm(12mil)	Plated	L1_TOP - L2_BOTTOM	Via	v30h12_t
☆	13	0.610mm(24mil)	Plated	L1_TOP - L2_BOTTOM	Via	v60h24
	100 Total					

Drill Table - pads

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
⊕	1	0.800mm(31mil)	Plated	L1_TOP - L2_BOTTOM	Pad	c130h80
⊕	1	0.800mm(31mil)	Plated	L1_TOP - L2_BOTTOM	Pad	s130h80m140
◇	15	1.020mm(40mil)	Plated	L1_TOP - L2_BOTTOM	Pad	c170h102
⊗	1	1.020mm(40mil)	Plated	L1_TOP - L2_BOTTOM	Pad	s170h102
□	4	1.600mm(63mil)	Plated	L1_TOP - L2_BOTTOM	Pad	c320h160
○	4	2.997mm(118mil)	Plated	L1_TOP - L2_BOTTOM	Pad	pad_corner
	26 Total					

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Drill tables & drill drawing

Engineer: T. Duris

Date: 12. May 2021 18:03

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