SECO-NCP51561XADW2G-GEVB Evaluation Board User's Manual

EVBUM2756/D

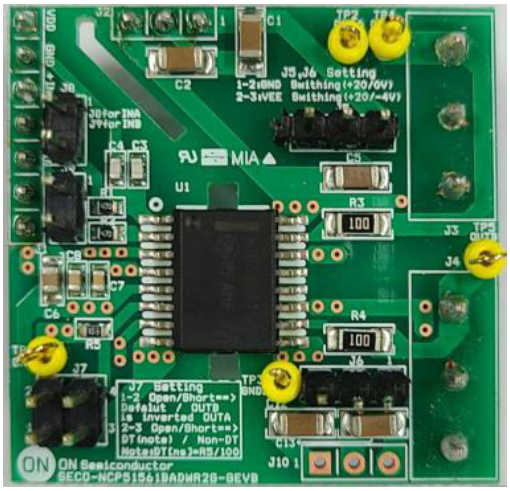


Figure 1. Evaluation Board Picture

Description

This user guide is applicable to the daughter cards of NCP51561. It should be used in conjunction with the NCP51561 datasheets as well as **onsemi**'s application notes and technical support team. Please visit **onsemi**'s website at at www.onsemi.com.

This document describes the proposed solution for 5 kV_{RMS} isolated dual channel gate driver using the NCP51561. This user's guide also includes information regarding operating procedures, input/output connections, an electrical schematic, printed circuit board (PCB) layout, and a bill of material (BOM) for the evaluation board.

This EVB can be used as a daughter card to be compatible with the SECO−GDBB−EVB gate drivers' baseboard, which allows testing simultaneously and comparing the performances. The connection with SECO−GDBB−EVB is mentioned in Figure 16.

These evaluation boards can be used to evaluate:

- NCP51561xyDWR2G
- NCV51561xyDWR2G
- NCP51560xyDWR2G
- NCP51563xyDWR2G
- NCV51563xyDWR2G

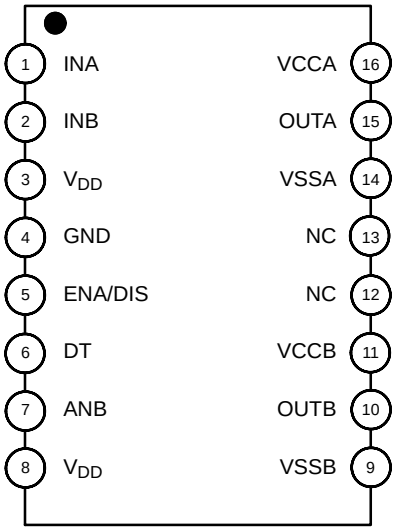
Collaterals

- SECO−NCP51561BADW2G−GEVB
- SECO−GDBB−GEVB
- NCP51560
- NCP51561
- NCP51563

Key Features

- Flexible: Dual Low−Side, Dual High−Side or Half−Bridge Gate Driver
- Independent UVLO Protections for Both Output Drivers
- Output Supply Voltage from 6.5 V to 30 V with 8 V, and 17 V UVLO Threshold
- 4.5 A Peak Source, 9 A Peak Sink Output
- 200 V/ns dV/dt Immunity
- 36 ns Typical Propagation Delay
- 5 ns Max Delay Matching
- User Programmable Input Logic
  - Single or Dual−input modes via ANB (NCP51561, NCP51563)
- User Programmable Dead−Time
- ENABLE or DISABLE Mode
- Isolation & Safety
  - 5 kV_{RMS} Isolation for 1 Minute (per UL1577 Requirements) and 1500 V Peak Differential Voltage between Output Channels
  - 8000 V_{PK} Reinforced Isolation Voltage (per VDE0884−11 Requirements)

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM

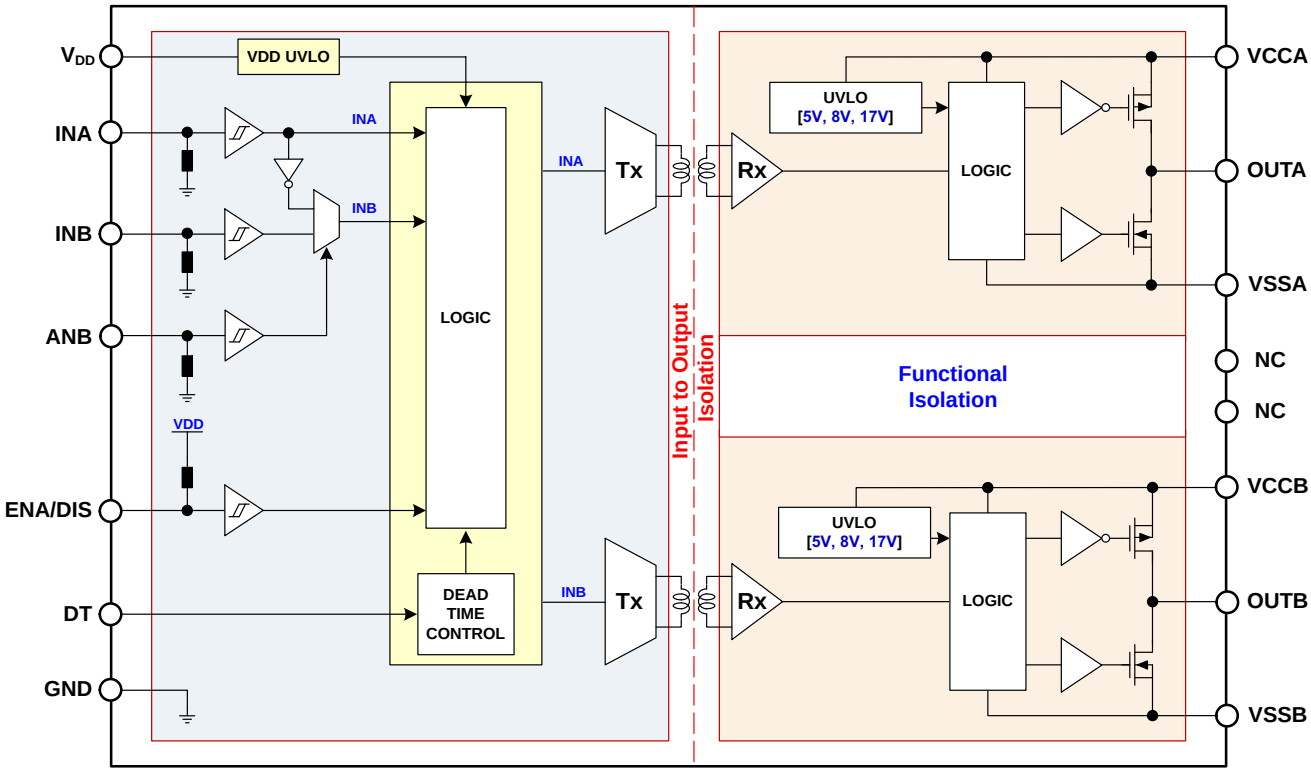


Figure 2. Functional Block Diagram

EVALUATION BOARD OPERATION

This section describes how to operate the NCP51561 evaluation board (EVB). Make external connections to the NCP51561 EVB using either the installed test−points or by installing wires into the connectors. The main connections that must be made to the EVB are the analog supply voltage, input signal, and output load and monitoring equipment.

Features

- Evaluation board for the NCP5156x product family in a wide body SOIC−16 package: NCP51561xyDWR2G, NCV51561xyDWR2G, NCP51560xyWR2G, NCP51563xyDWR2G and NCV51563xyDWR2G
- 3−V to 5.0−V VDD power supply range, and up to 30−V VCCA/VCCB power supply range
- 4−A and 8−A source/sink current driving capability
- 5−kV$_{RMS}$ Isolation for 1 minute per UL 1577
- TTL −compatible inputs
- Allowable input voltage up to 18−V with for INA, INB, and ANB pins
- On−board trimmer potentiometer for dead−time programming
- Jumper option to be compatible with the SECO−GDBB−EVB
- Support for half−bridge test with MOSFETs, IGBTs and SiC MOSFETs with connection to external power stage

Power and Ground

Note: Connecting the all power supplies in reverse polarity (backwards) will instantly device when power is turned on and device damage can result.

The primary side of the EVM (V_{DD}) operates from a single 3−V to 5.0−V power supply and connected via J2.

The EVM provides connections for evaluating the output side (V_{CCA}, V_{SSA}, V_{CCB}, and V_{SSB}) power supplies for the channel A and B, from a minimum 6.5−V to maximum 30−V for 5−V UVLO version as shown in Figure 3. VCCA and VCCB can be monitored via TP9 and TP13, respectively.

The V_{CCA} and V_{CCB} pin should be bypassed with a capacitor with a value of at least ten times the gate capacitance, and over 100 nF and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. We had recommends using 2 capacitors; a over 100 nF ceramic surface−mount capacitor, and another a tantalium or electrolytic capacitor of few microfarads added in parallel.

Input and Output

1. Connection of primary−side power supply to the V_{DD} connector [J1].
2. Connection of secondary−side power supply to the V_{CCA} and V_{CCB} connector [J2 and J10].
3. Connection of INA signal to the SIGNAL connector [J1].
4. Connection of INB signal to the SIGNAL connector [J1].
5. Connection of jumpers to set INPUT stage [J8 and J9].
6. Connection of ANB pin via ANB jumper [J7].
7. Connection of DT pin via DT jumper [J7].
8. Connection of MOSFET of IGBT to the OUT connector [J3 and J4].
9. Connection of jumpers to set OUTPUT stage [J5, J6, J10 and J11].

*The setting of jumpers are mentioned in Table 2.

Schematics of Evaluation Board

Figure 3 shows an application schematic of NCP51561 EVB.

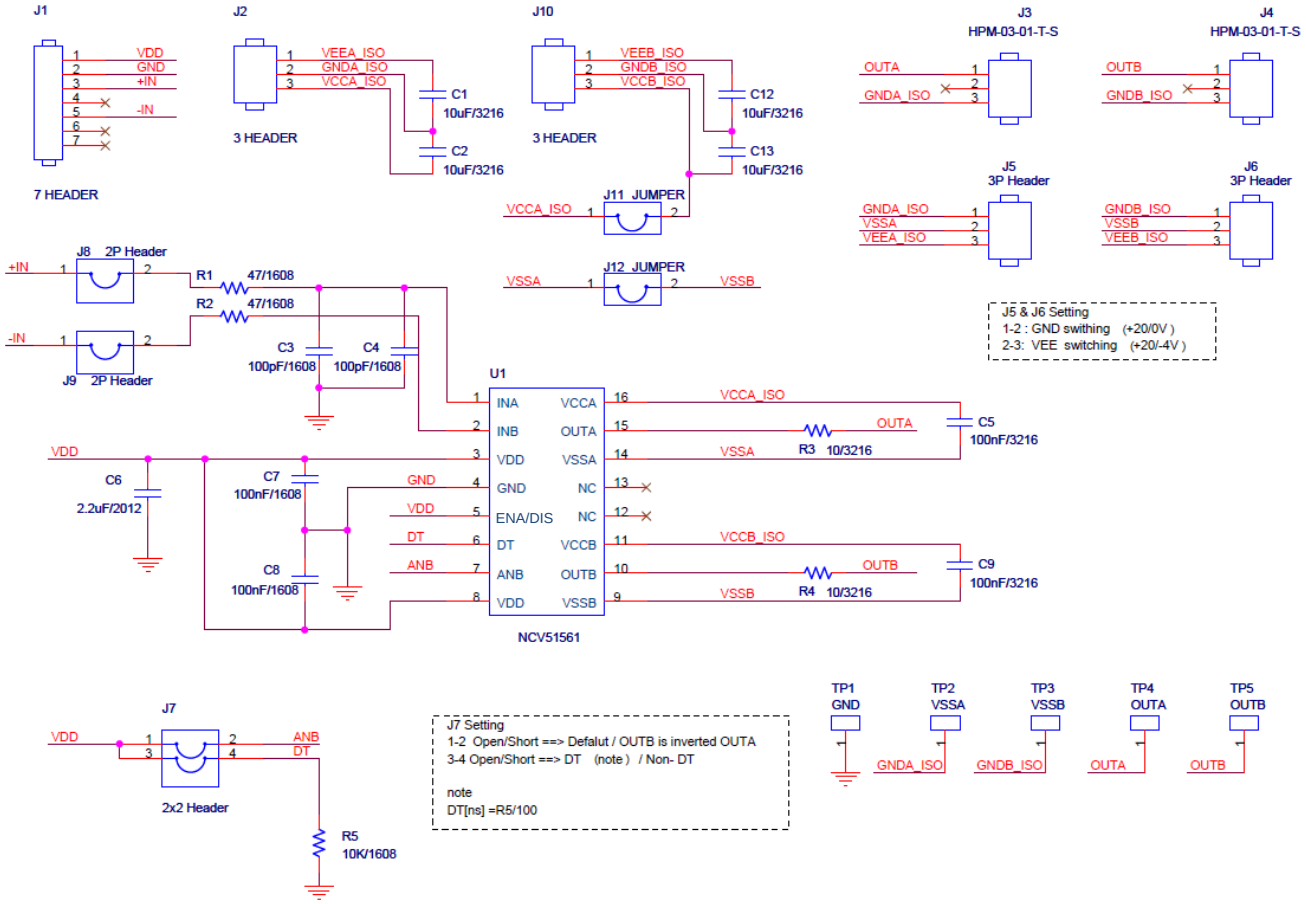


Figure 3. Schematic of NCP51561 EVB

List of Test Points

Table 1 shows the list of test points in the evaluation board.

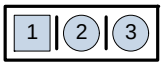
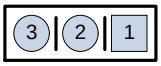
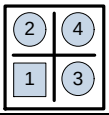
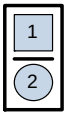
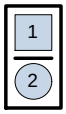
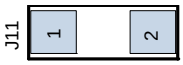
Table 1. LIST OF TEST POINTS

TP #	Reference	Description
TP1	GND	Ground Input−side (all signals on input−side are referenced to this pin)
TP2	VSSA	Ground for Channel A
TP3	VSSB	Ground for Channel B
TP4	OUTA	Output for Channel A
TP5	OUTB	Output for Channel B

Position of Jumpers

Table 2 shows the position of jumpers in the evaluation board.

Table 2. POSITION OF JUMPERS

Ref #	Feature	Position	Description	Default Setting
J5	J5 	1−2	GND switching (+20/0 V)	Short
		2−3	VEE switching (+20/−4 V)	Open
J6*	J6 	1−2	GND switching (+20/0 V)	Open
		2−3	VEE switching (+20/−4 V)	Open
J7	J7 	1−2	Open: Normal Mode (INA → OUTA, INB → OUTB) Short: OUTB is inverted OUTA	Open
		3−4	Open: Deadtime (DT[ns] = R5/100) Short: Non−Deadtime	Open (DT = 100 ns)
J8	J8 	1−2	Open: +IN disconnection Short: +IN connection	Short
J9	J9 	1−2	Open: −IN disconnection Short: −IN connection	Short
J11		1−2	Open: Disconnection between VCCA and VCCB Short: Connection between VCCA and VCCB	Short
J12		1−2	Open: Disconnection between VCCA and VCCB Short: Connection between VSSA and VSSB	Short

*J6 is not applicable to be compatible with the SECO−GDBB−EVB because J5 setting affect both OUTA and OUTB. But user can utilize J6 for stand−alone operation without SECO−GDBB−EVB.

I/O Connectors

Table 3 shows the description of external connectors.

Table 3. DESCRIPTION OF CONNECTOR'S PIN

Ref.	Pin #	Name	Type	Description
J1	1	VDD	Power	Input−side Supply Voltage.
	2	GND	Power	Ground Input−side. (all signals on input−side are referenced to this pin)
	3	+IN	Input	Logic input for Channel A
	4	Not used	NA	NA
	5	−IN	Input	Logic input for Channel B
	6	Not used	NA	NA
	7	Not used	NA	NA
J2	1	VEEA ISO	Power	Isolated negative voltage supply for Channel A
	2	GNDA ISO	Power	Isolated GND for Channel A
	3	VCCA ISO	Power	Isolated supply voltage for Channel A
J3	1	OUTA	Out	Output for Channel A
	2	Not used	NA	NA
	3	GNDA ISO	Power	Isolated GND for Channel A
J4	1	OUTB	Out	Output for Channel B
	2	Not used	NA	NA
	3	GNDB ISO	Power	Isolated GND for Channel B
J5	1	GNDA ISO	Power	Isolated GND for Channel A
	2	VSSA	Power	GND for Channel A
	3	VEEA ISO	Power	Isolated negative voltage supply for Channel A
J6	1	GNDB ISO	Power	Isolated GND for Channel B
	2	VSSB	Power	GND for Channel B
	3	VEEB ISO	Power	Isolated negative voltage supply for Channel B
J10	1	VEEB ISO	Power	Isolated negative voltage supply for Channel B (NA for SECO−GDBB−EVB)
	2	GNDB ISO	Power	Isolated GND for Channel B (NA for SECO−GDBB−EVB)
	3	VCCB ISO	Power	Isolated supply voltage for Channel B (NA for SECO−GDBB−EVB)

Electrical Specifications

Table 4 shows the recommended operating conditions of NCP51561 EVB.

Table 4. ELECTRICAL CHARACTERISTICS

Rating		Symbol	Min.	Max.	Unit
Power Supply Voltage – Input side		V_{DD}	3.0	5.0	V
Power Supply Voltage – Driver side	5−V UVLO Version (NCP5156XAA)	V_{CCA}, V_{CCB}	6.5	30	V
	8−V UVLO Version (NCP5156XBA)		9.5	30	V
	17−V UVLO Version (NCP5156XDA)		18.5	30	V
Logic Input Voltage at pins INA, INB, and ANB		V_{IN}	0	18	V
Logic Input Voltage at pin ENA/DIS		$V_{ENA/DIS}$	0	5.0	V
Operating Junction Temperature		Tj	−40	+150	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Bill of Material (BOM)

Table 5 shows the bill of material (BOM) of NCP51561 EVB.

Table 5. BILL OF MATERIAL (BOM)

#	Ref.	Part No.	Definition	Q'ty	Manufacturer
1	C1, C2	CL31B106KBHNNNE	10 μF, 50 V, X7R	2	SAMSUNG ELEC.
2	C3, C4	CL03C010BA3GNNC	1 nF, 25 V, NPO	2	SAMSUNG ELEC.
3	C5, C9	CL31B104KBCNNNC	100 nF, 50 V, X7R	2	SAMSUNG ELEC.
4	C6	CL21B225KAFNNNE	2.2 μF, 25 V, X7R	1	SAMSUNG ELEC.
5	C7, C8	CL10B104MO8NNND	0.1 μF, 25 V, X7R	2	SAMSUNG ELEC.
6	J1	A2−7PA−2.54DSA	7 HEADER	1	Hirose
7	J2	A2−3PA−2.54DSA	3 HEADER	1	Hirose
8	J3, J4	HPM−03−01−T−S	5.08 mm Connector	2	Samtec
9	J5, J6	A2−3PA−2.54DSA	3P Header	2	Hirose
10	J7	A1−4PA−2.54DSA	2x2 Header	1	Hirose
11	J8, J9	A2−2PA−2.54DSA	2P Header	2	Hirose
12	J10*	A2−3PA−2.54DSA	2.54 mm 3P	1	Hirose
13	J11, J12	S1731−46R	2P Shorting pin, 6.86 mm	2	HARWIN
14	R1, R2	ESR03EZPJ470	47 Ω, 5%, 1/4 W	2	Rohm
15	R3, R4	MCR18EZPJ100	10 Ω, 5%, 1/4 W	2	Rohm
16	R5	ESR03EZPJ102	1 kΩ, 5%, 1/4 W	1	Rohm
17	TP1, TP2, TP3, TP4, TP5	3082	Test Point, 1 mm hole	10	Young−Jin Enterprise
18	U1	NCV51561		1	ON Semiconductor

*J10 is not soldered to be compatible with the SECO−GDBB−EVB. User can utilize this connector for stand−alone operation without SECO−GDBB−EVB.

INPUT STAGE

The input pins of NCP51561 is based on a TTL compatible input−threshold logic that is independent of the V_{DD} supply voltage for INA, INB, ANB, and ENA/DIS pins.

The logic level compatible input provides a typically high threshold of 1.7 V and a typically low threshold of 1.1 V. The input impedance of the NCP51561 is 200 kΩ typically, as shown in Figure 4.

And we recommends an RC network is to be added on the PWM input pins, INA and INB, for reducing the impact of system noise and ground bounce, for example, 47 Ω (R1, and R2) with 100 pF (C1, and C2) is applied to NCP51561 EVB as shown in Figure 4.

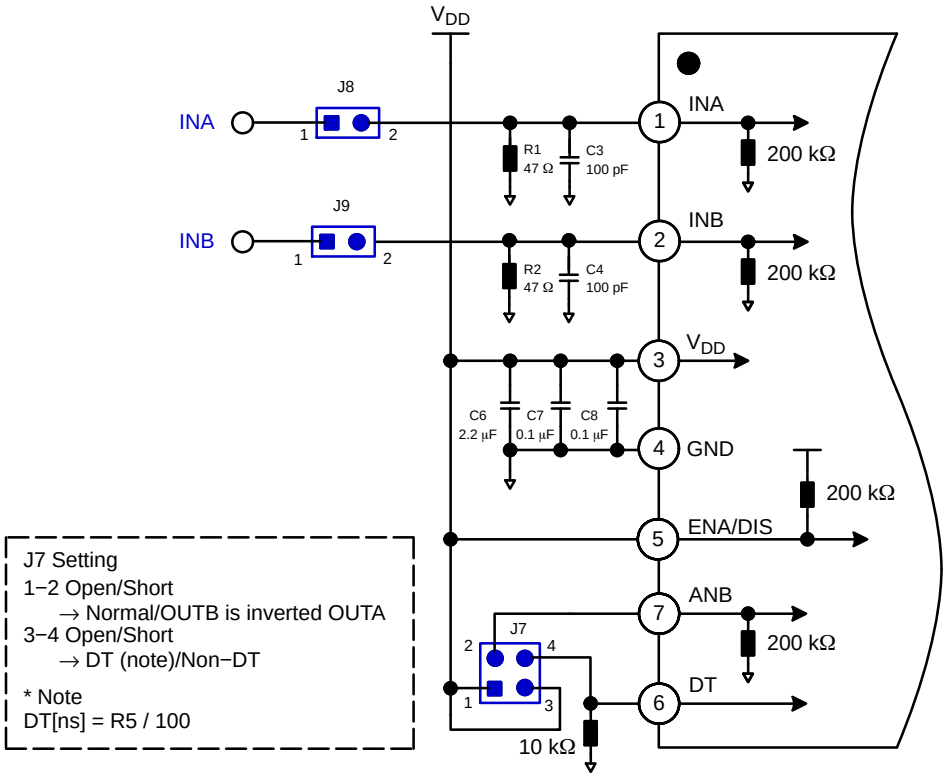


Figure 4. Input Circuit of NCP51561 EVB

OUTPUT STAGE

The output stage is able to sink/source typically around 4.0 A/8 A at 25°C for the NCP51561.

The EVB comes populated with a 1 nF load (C5, and C11) on the output side.

The EVB also allows for evaluation of the device with an MOSFET load in either of the standard TO−220, TO−3P and TO−247. The OUTA and OUTB can be monitored directly via TP4 and TP5, respectively.

PERFORMANCE OF EVALUATION BOARD

This section describes application guidance and operation of the NCP51561 for an evaluation board (EVB) include key functions.

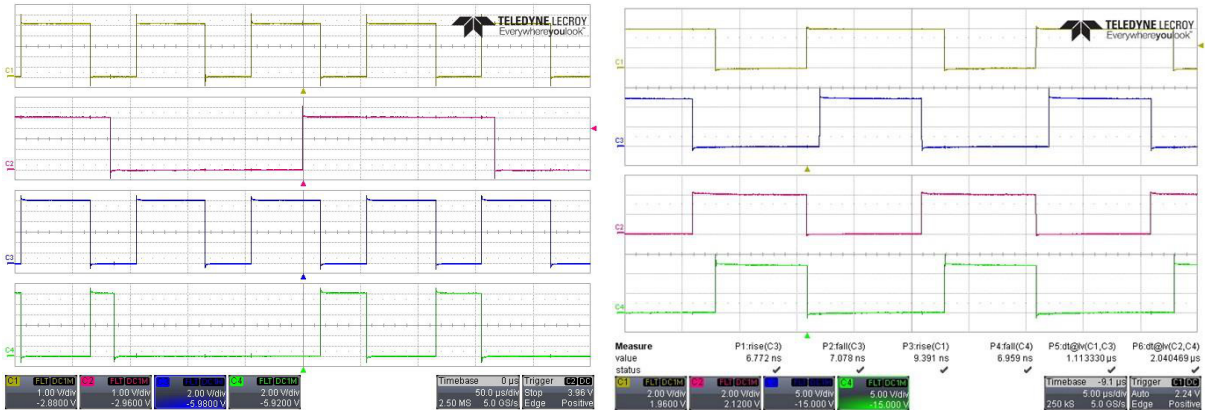
Input Signal Configuration

The NCP51561 allows changing the input signal pin configuration by the ANB pin for user convenience. (e.g. single input – dual output, or dual input – dual output).

ANB Function

The NCP51561 allows changing the input signal pin configuration by the ANB pin for user convenience. There are two operating modes that allow changing the configuration of the input to output channels (e.g. single input – dual output, or dual input – dual output).

Figure 5 and Figure 6 shows the experimental result of ANB function with and without dead−time control.

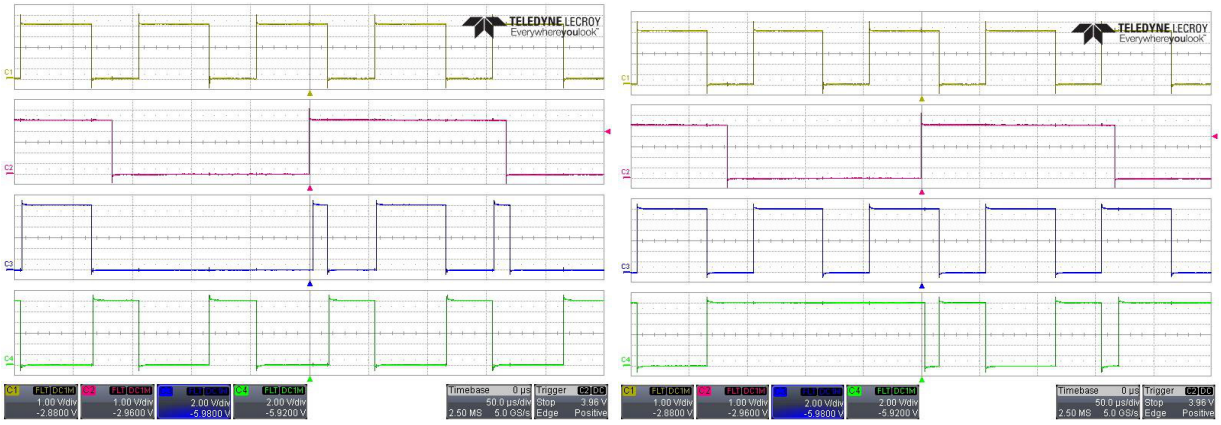


(a) INB = OPEN (LOW) with DT = Open

(b) INB = OPEN (LOW) with R_{DT} = 100 kΩ

CH1: INA, CH2: ANB, CH3: OUTA, and CH4: OUTB

Figure 5. Experimental Waveforms of ANB Function with Dead−time



(a) INB = HIGH with DT = Open

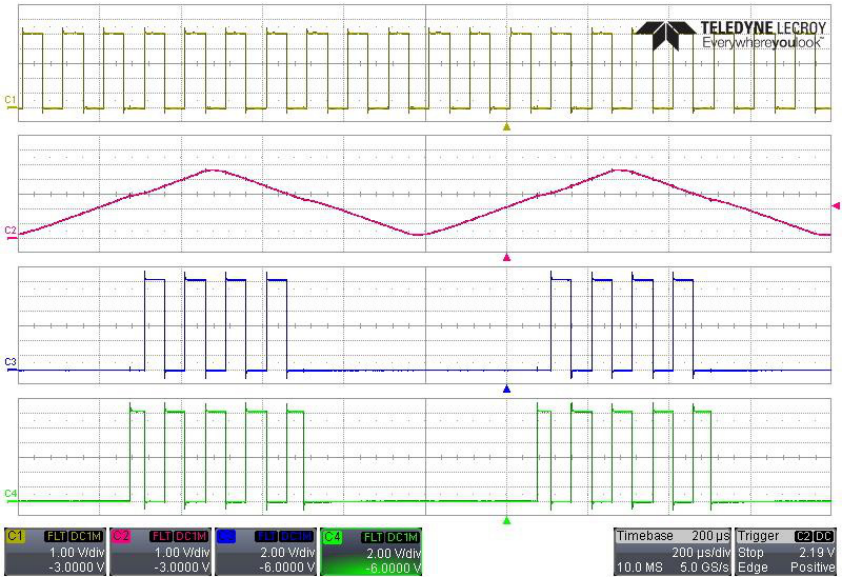
INB = HIGH with DT = V_{DD}

CH1: INA, CH2: ANB, CH3: OUTA, and CH4: OUTB

Figure 6. Experimental Waveforms of ANB Function

Under−Voltage Lockout Protection VDD

The NCP51561 provides the Under−Voltage Lockout (UVLO) protection function for VDD in primary−side as shown in Figure 7. The OUTA and OUTB as complementary outputs from one PWM input signal on the INA pin regardless the INB signal when the ANB pin is high. As test result, the VDD UVLO turn−on and off threshold voltages are around 2.8 V and 2.7 V respectively.

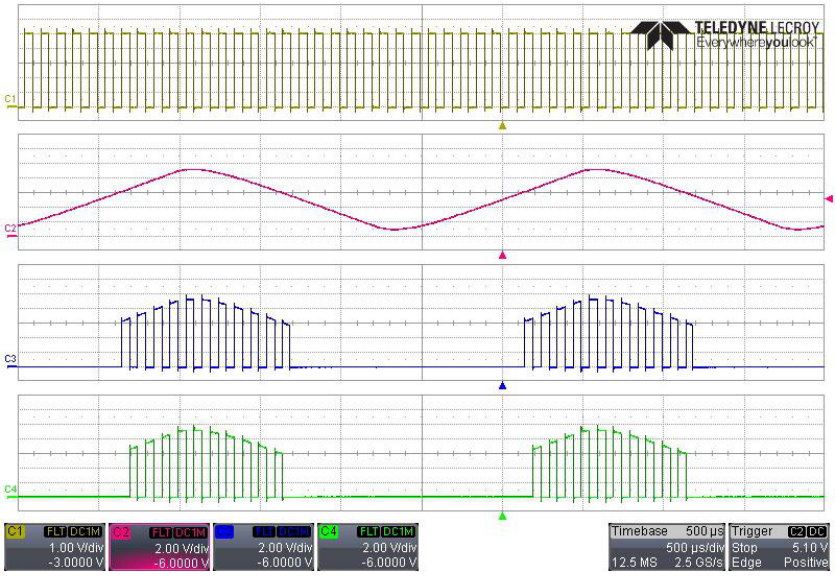


CH1: INA, CH2: VCCA and VCCB, CH3: OUTA, and CH4: OUTB

Figure 7. Experimental Waveforms of VDD Under−Voltage Lockout Protection

Under−Voltage Lockout Protection VCCx (VCCA and VCCB)

The NCP51561 provides the Under−Voltage Lockout (UVLO) protection function for both gate drive output for VCCA and VCCB for 5−V version in secondary−side as shown in Figure 8. The OUTA and OUTB as complementary outputs from one PWM input signal on the INA pin regardless the INB signal when the ANB pin is high. As test result, the VCC UVLO turn−on and off threshold voltages are around 6.0 V and 5.7 V respectively.



CH1: INA, CH2: VCCA and VCCB, CH3: OUTA, and CH4: OUTB

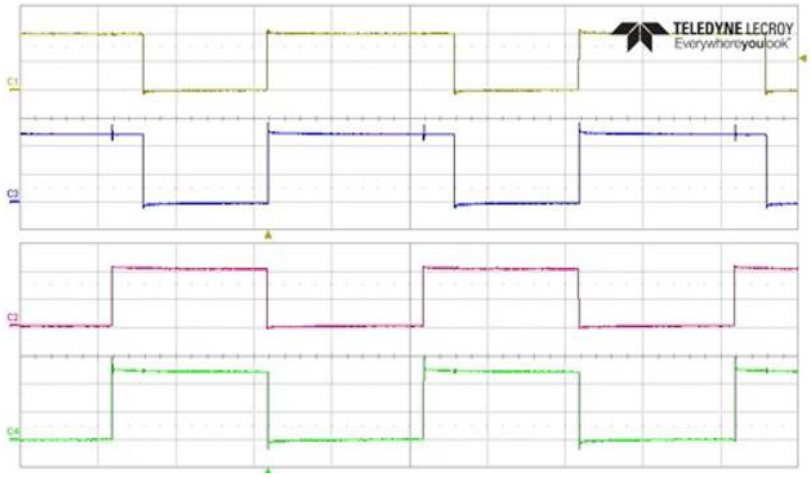
Figure 8. Experimental Waveforms of VCC Under−Voltage Lockout Protection

Experimental Waveforms with Different DT Configurations

This section shows experimental test results of dead−time control with different DT configuration.

DT Pin Connected to VDD (Short status on J7 3−4 in Table 2)

Overlap is allowed both switches from conducting even though at the same time when the DT pin pulled to VDD as shown in Figure 9.



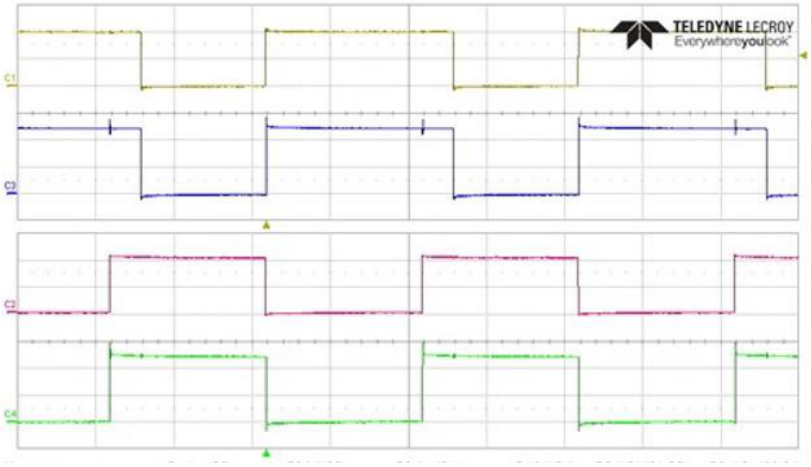
CH1: INA, CH2: INB, CH3: OUTA, and CH4: OUTB

Figure 9. Overlap is Allowed when DT Connected to VDD

DT Pin Connected to RDT
(Open status on J7 3−4 in Table 2)

Overlab is not allowed both switches at the same time when the dead time (DT) control mode. The dead−time (DT) between both outputs is set according to: DT (in ns) = 10 × R_{DT} (in kΩ).

Figure 10 shown the experimental results when the dead−time control resistance for 100 kΩ.



CH1: INA, CH2: INB, CH3: OUTA, and CH4: OUTB

Figure 10. Experimental Waveforms if DT Connected to R_{DT}

Dead Time Characteristics

Figure 11 shows the dead time characteristics and operating modes according to the dead−time resistance values of the NCP51561.

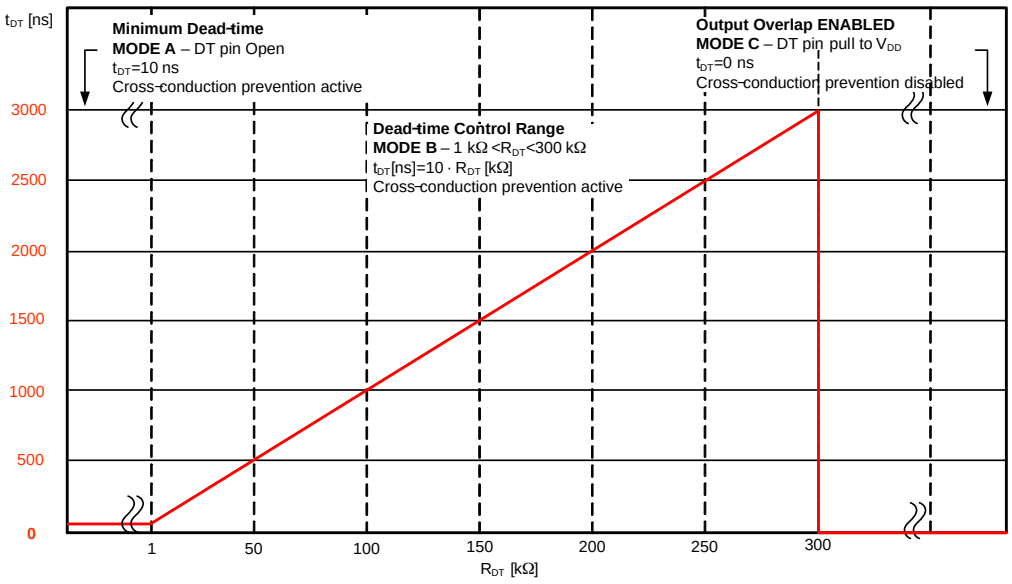
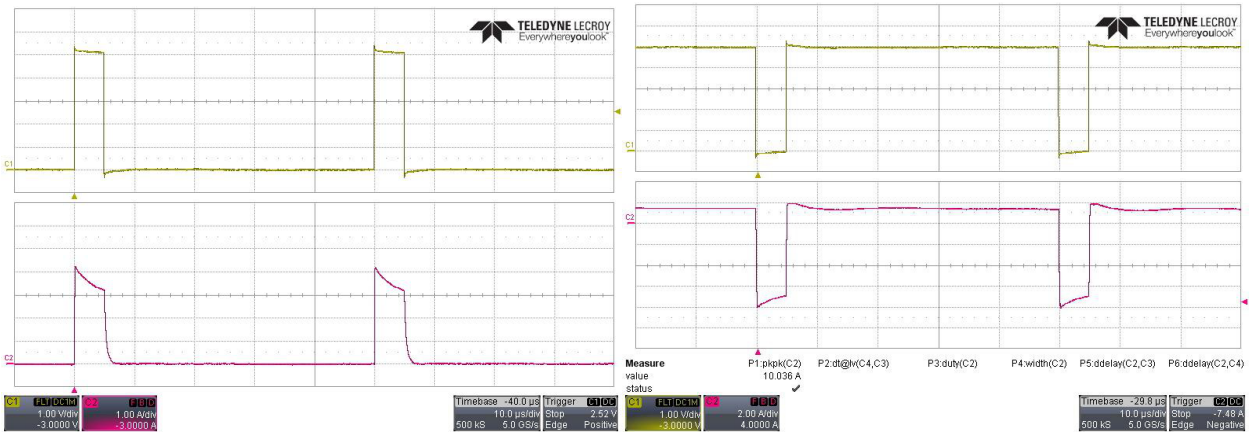


Figure 11. Dead Time (DT vs. R_{DT})

Output Driving Current Capability

Figure 12 shows the experimental result of source and sink peak currents driving capability around 4.0 A and 10 A respectively at 25°C when the supply voltage (VCCA and VCCB) is applied 12 V.



(a) Source Current Capability (b) Sink Current Capability

CH1: INPUT, and CH2: OUTPUT Current

Figure 12. Experimental Waveforms of Current Driving Capability

ESD Structure

Figure 13 shows the multiple diodes related to an ESD protection components of NCP51561. This illustrates the absolute maximum rating for the device.

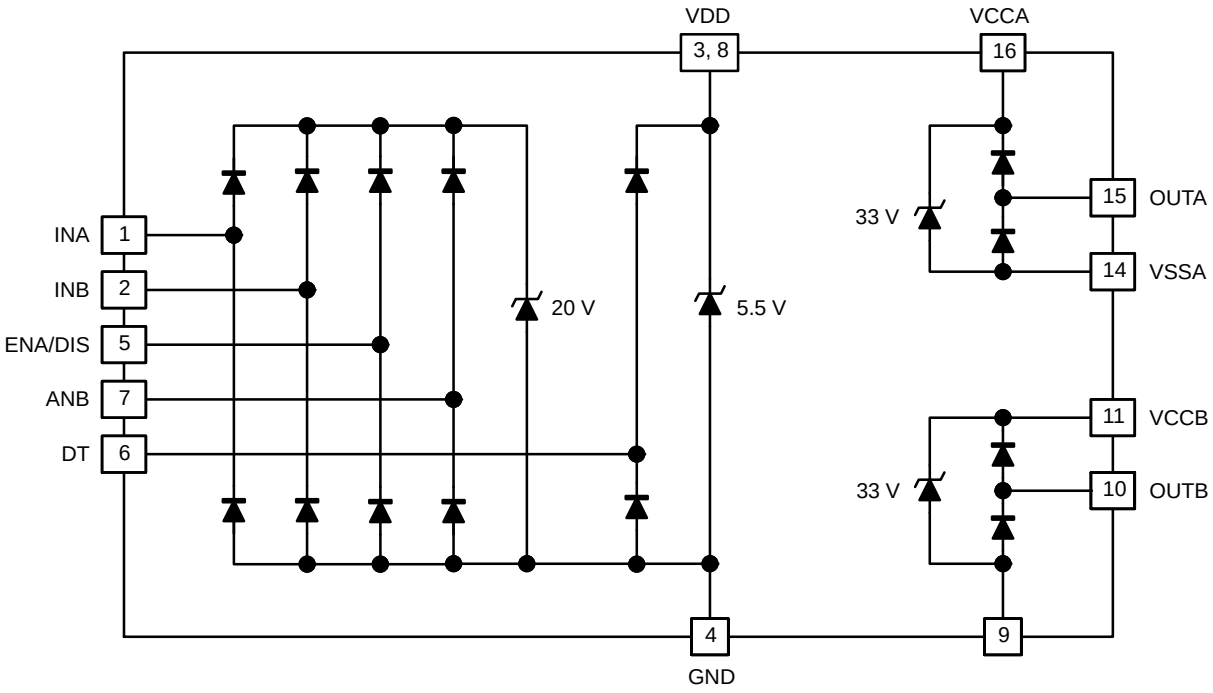


Figure 13. ESD Structure

Printed Circuit Board

Figure 14 shows the photograph of NCP51561 evaluation board.

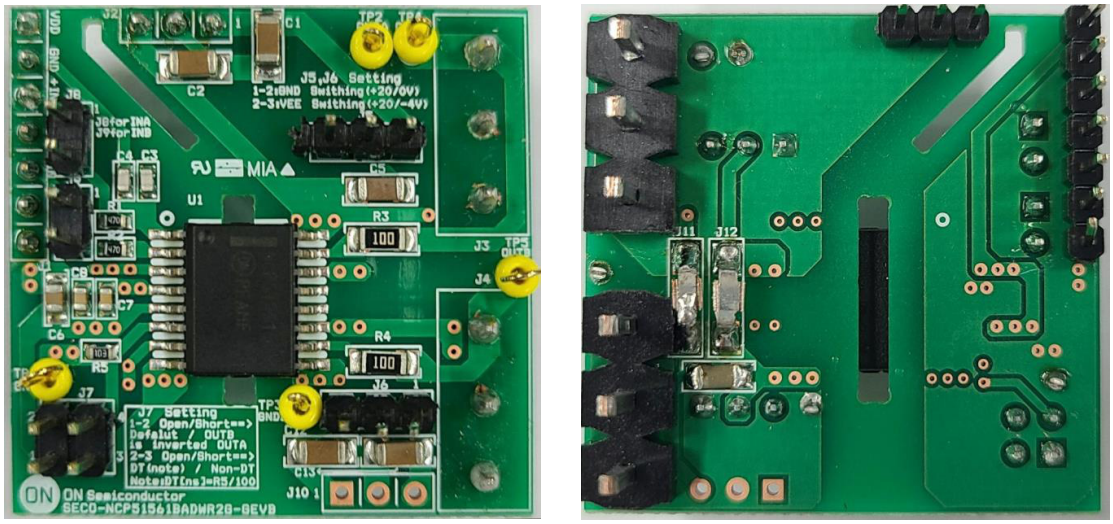
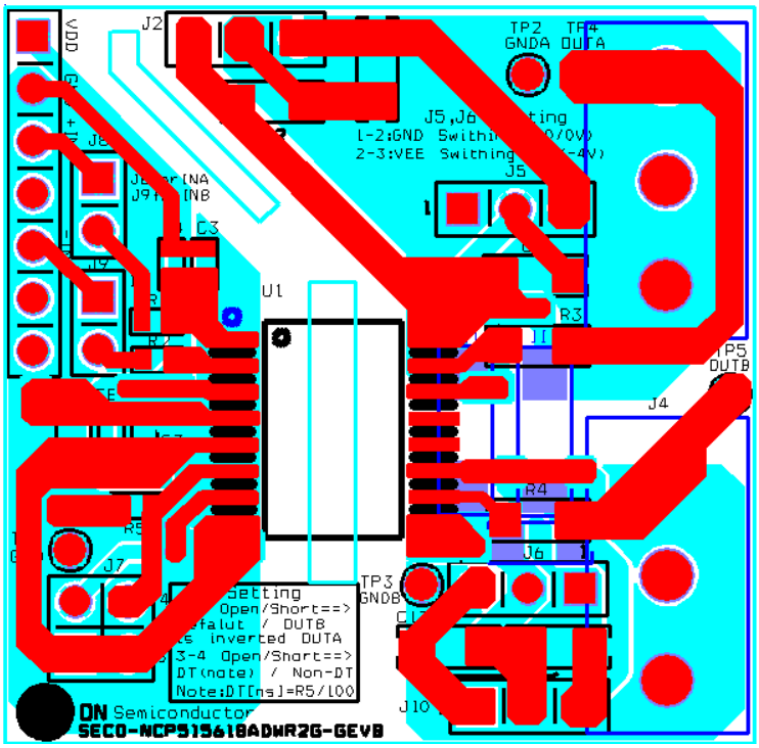
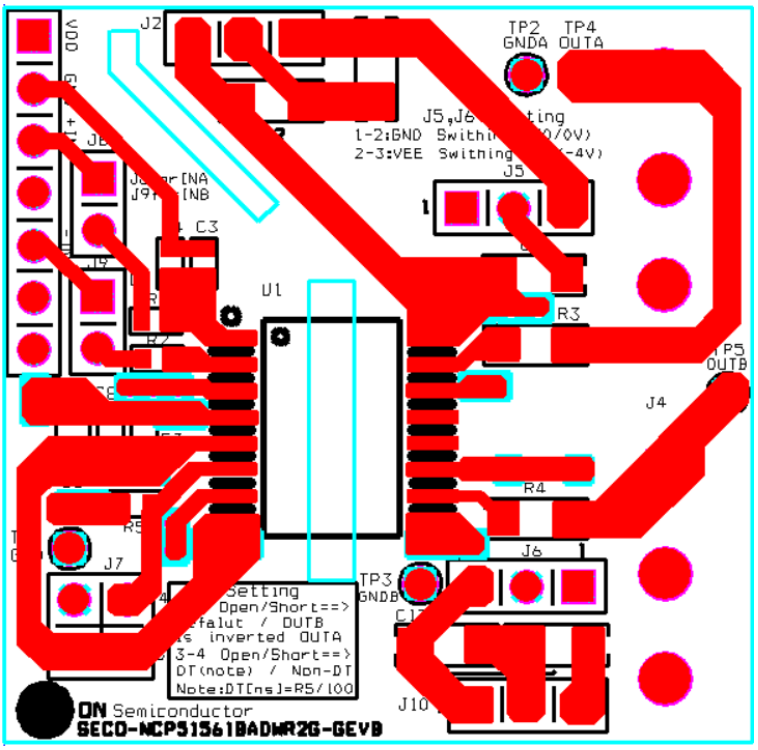


Figure 14. Evaluation Board Picture (Top & Bottom View)

Figure 15 shows the printed circuit board layout of NCP51561 evaluation board.

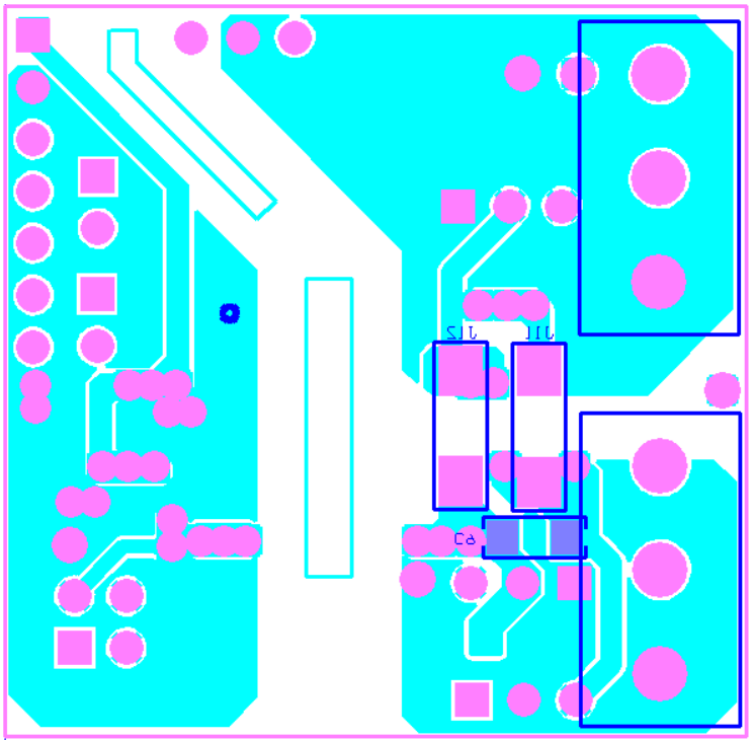


(a) Top & Bottom View



(b) Top View

Figure 15. Printed Circuit Board (Part 1)



(b) Top View

Figure 15. Printed Circuit Board (Part 2)

Figure 16 shows the connection of NCP51561 EVB as an daughter card of SECO−GDBB−EVB.

Figure 16. Connection with SECO−GDBB−EVB

Test Configuration

Figure 17 shows the example how to measure output signals with using Mother Board (SECO−GDBB−EVB).

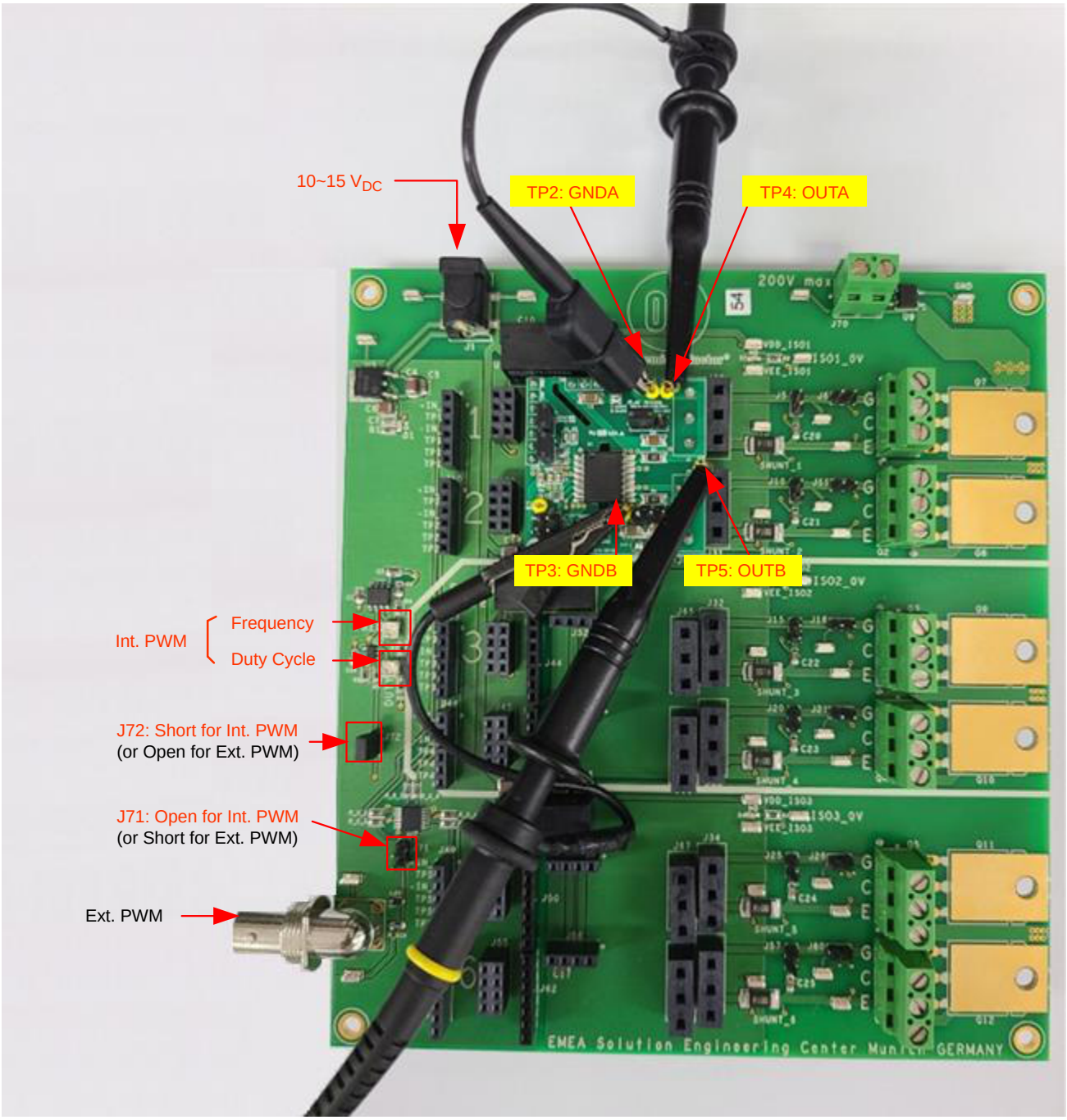
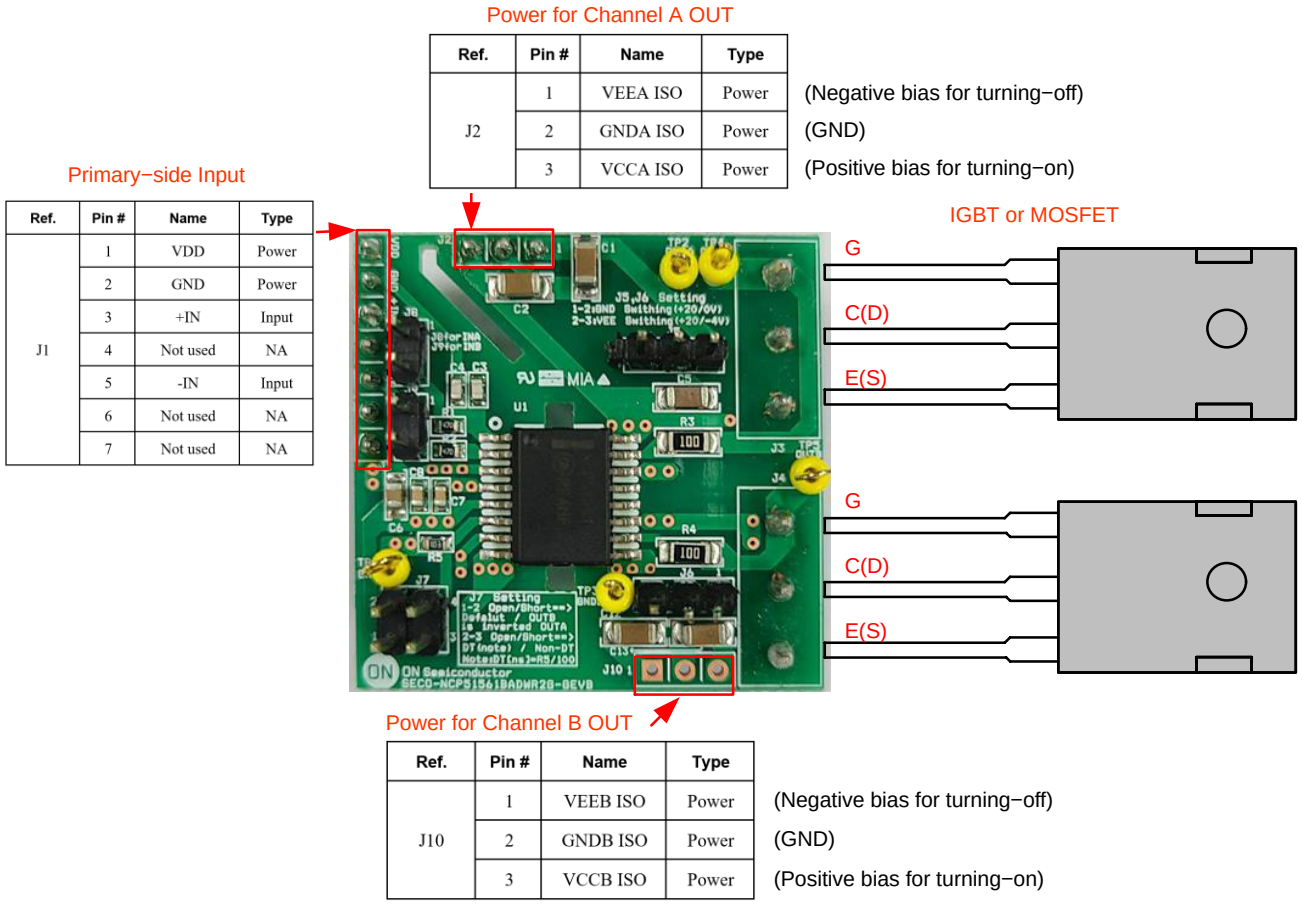


Figure 17. Example for Measuring OUT Signals with using Mother Board (SECO−GDBB−EVB)

Figure 18 shows the example how to utilize the EVB without Mother Board (SECO−GDBB−EVB).



Ref.	Pin #	Name	Type
J2	1	VEEA ISO	Power
	2	GNDA ISO	Power
	3	VCCA ISO	Power

(Negative bias for turning−off)
(GND)
(Positive bias for turning−on)

Ref.	Pin #	Name	Type
J1	1	VDD	Power
	2	GND	Power
	3	+IN	Input
	4	Not used	NA
	5	-IN	Input
	6	Not used	NA
	7	Not used	NA

Ref.	Pin #	Name	Type
J10	1	VEEB ISO	Power
	2	GNDB ISO	Power
	3	VCCB ISO	Power

(Negative bias for turning−off)
(GND)
(Positive bias for turning−on)

Figure 18. Test Configuration of EVB without Mother Board (SECO−GDBB−EVB)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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