AP0101_81BGA_Adapter_Rev2

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4	Power
5	Clock and Reset
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8	FPGA Interface
9	Configuration Setting

Rev	Who	Date	Description
Rev 0.0	W.B.Foo	06/20/11	Initial.
Rev 0.1	W.B.Foo	08/18/11	Add P5, P51 and P19
Rev 0.2	W.B.Foo	08/19/11	Add U20, R63, Q1 and change P29 to polarized type type connector
Rev 0.3	W.B.Foo	08/23/11	Add P30, P31, P52, P53, R63, Q2, Q3, P8 and R55
Rev 1.0	W.B.Foo	10/10/11	Change Level Translator U11/U12 from PCA9517 to TXB0102 & R24/R25 to 2.2K resistor on Pg 5
Rev 1.1	W.B.Foo	10/28/11	Change test point TP6/TP7/TP8/TP11/TP10 to through hole type
Rev 1.2	W.B.Foo	12/19/11	1) Change U16/U24 to single part of U24(SN74AVCH4T245) combine M_TRIG/MCLK_OUT/RST_N_OUT 2) Add power supply for FPGA +1V2_VCCINT/+2V5_VCCA/+VCCIO/+3V3_HVCCIO 3) Add FPGA U32 & Flash Memory U47 4) Change P29 to smallest dimension type connector 5) Change U21 to TXB0102DCUR and add AND gate logic U27 SN74LVC1G08 FOR Auto-Config Circuit
Rev 1.3	W.B.Foo	01/30/12	1) Add external signal access for FRAME_SYNC 2) Change U31 AP0101 Symbol to non socket type
Rev 1.4	W.B.Foo	02/06/12	Add feedback resistor (R86) for XTAL (Y3)
Rev 1.5	W.B.Foo	02/22/12	Change U11 & U12 from TXB0102DCUR to TXS0102DCUR
Rev 2.0	W.B.Foo	04/25/12	Initial. 1) Change net name of U7 pin 5 VDDREG_ADJ to VCCINT_ADJ 2) Change U47 from N25Q128A13ESF40F to M25P64
Rev 2.1	W.B.Foo	05/03/12	Change SMPTE from J5 pin 15 to J6 pin 10 to support full PIXCLK of 20bit mode
Rev 2.2	W.B.Foo	05/08/12	Add Serial EEPROM (U16) on Host serial

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Title: <Title>		
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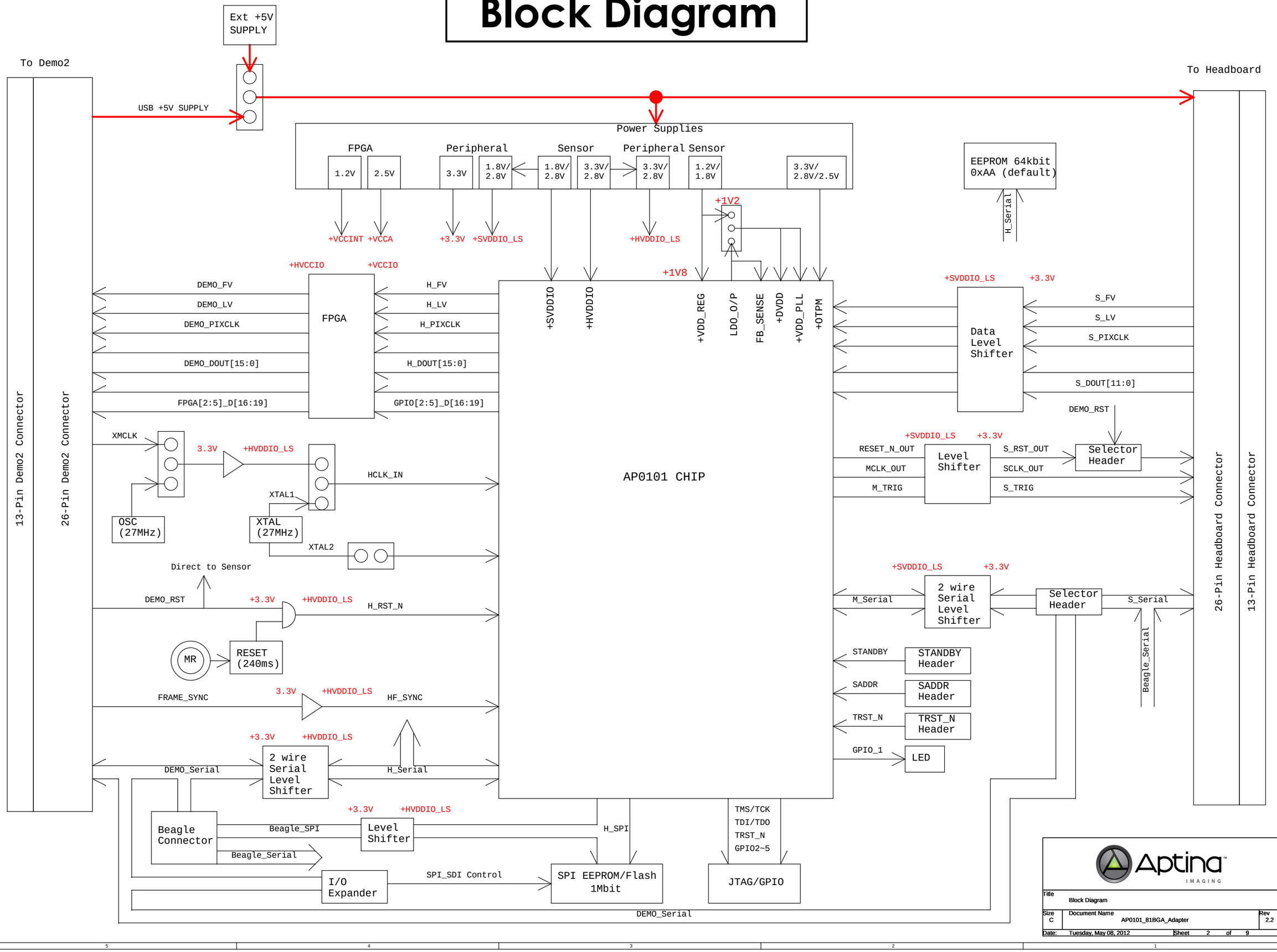
Block Diagram



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Title	Block Diagram	
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AP0101 IC

P19:
Short 1-2 (Default)

P19:
Close -> Default

P4 (SADDR):
Pins 2-3(GND) I2C Addr --> 0x90 (default)
Pins 1-2(+HVDDIO) I2C Addr --> 0xBA

P6 (STANDBY) Tri-stage:
Pins 2-3(GND) --> Standby mode
Pins 1-2(+3V3) --> Active mode (default)
Open -> Auto Control by serial

P3:
Short 2-3 (Default)

P8 (GPIO1_LED):
Pins 2-3 --> Set to GPO
Pins 1-2 --> Set to GPI

P7 (SPI Memory Selection):
Jumper 2-3 -> FLASH disable
Jumper 1-2 -> EEPROM disable

HOST Mode**(Default)**
P5 = Short 1-2/P45 = Open => SPI_SDI = GND

FLASH Mode
P5 = Open/P45 = Open => SPI_SDI = Flash/EEPROM Data

AUTO Config Mode
P5 = Short 1-2/P45 = Short 1-2 => SPI_SDI = High Impedance

Serial Control
P5 = Open/P45 = Open => SPI_SDI = Serial control mode type

SPI EEPROM
(1Mbit)

SPI FLASH
(512Kbit)

DIGITAL IMAGE
SENSOR

SPI PROGRAMMING CONNECTOR

Device Address:0x82

Title	AP0101 IC	
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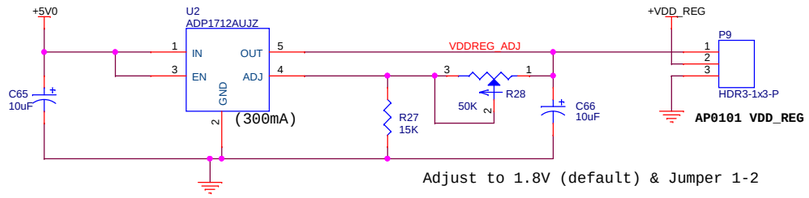
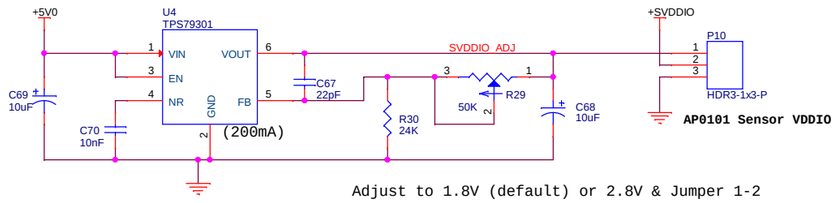
Power

VDD_REG 1.8V SUPPLY



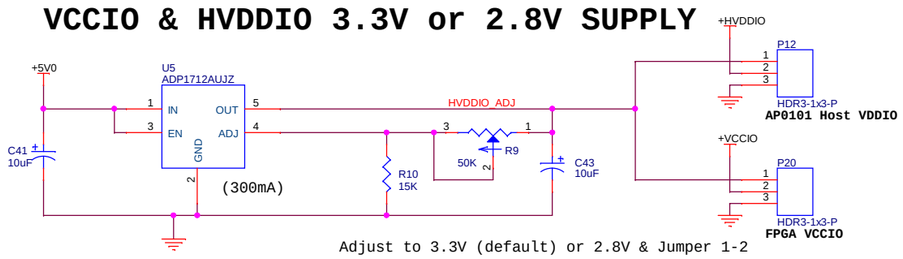
Adjust to 1.8V (default) & Jumper 1-2

SVDDIO 1.8V or 2.8V SUPPLY



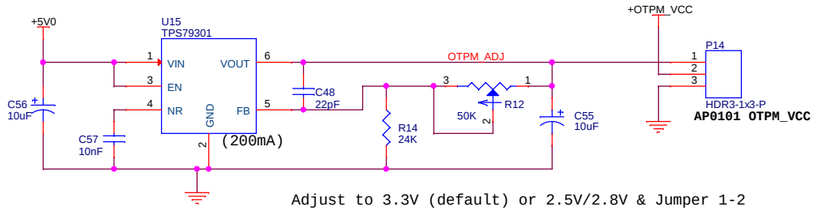
Adjust to 1.8V (default) or 2.8V & Jumper 1-2

VCCIO & HVDDIO 3.3V or 2.8V SUPPLY



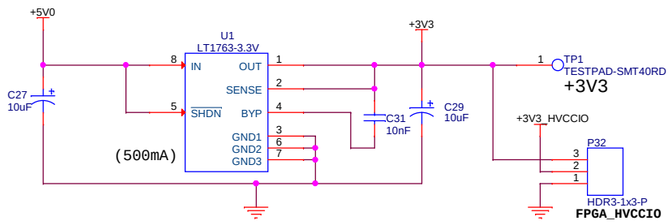
Adjust to 3.3V (default) or 2.8V & Jumper 1-2

VDD_OTPM 3.3V, 2.8V or 2.5V SUPPLY

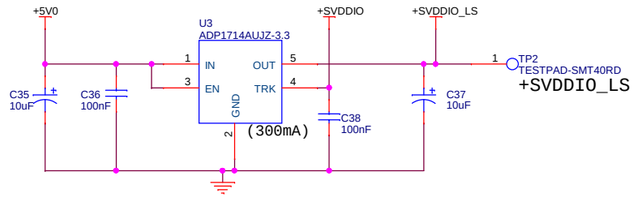


Adjust to 3.3V (default) or 2.5V/2.8V & Jumper 1-2

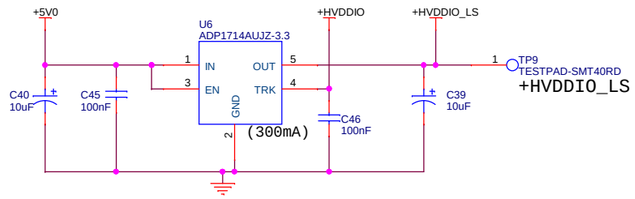
PERIPHERAL 3.3V SUPPLY



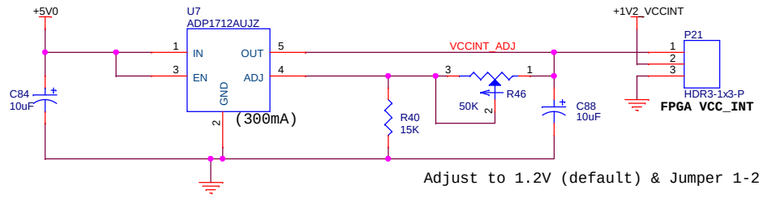
PERIPHERAL SVDDIO_LS SUPPLY



PERIPHERAL HVDDIO_LS SUPPLY

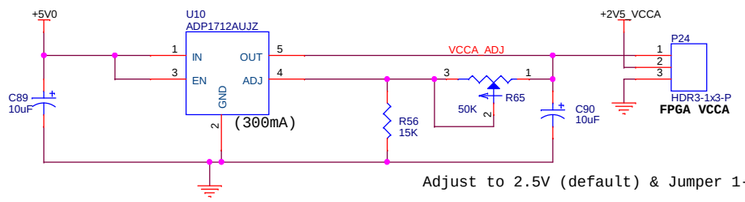


VCCINT 1.2V SUPPLY



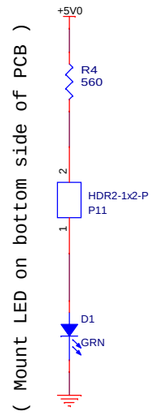
Adjust to 1.2V (default) & Jumper 1-2

VCCA 2.5V SUPPLY

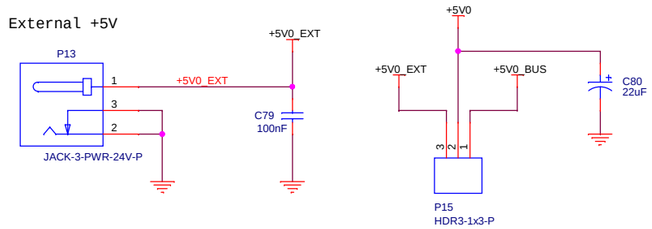


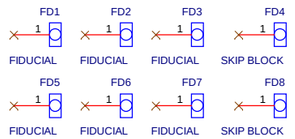
Adjust to 2.5V (default) & Jumper 1-2

5V LED

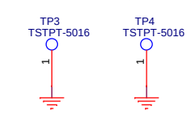


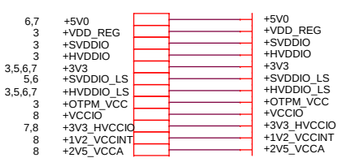
External +5V





Ground Testpoints





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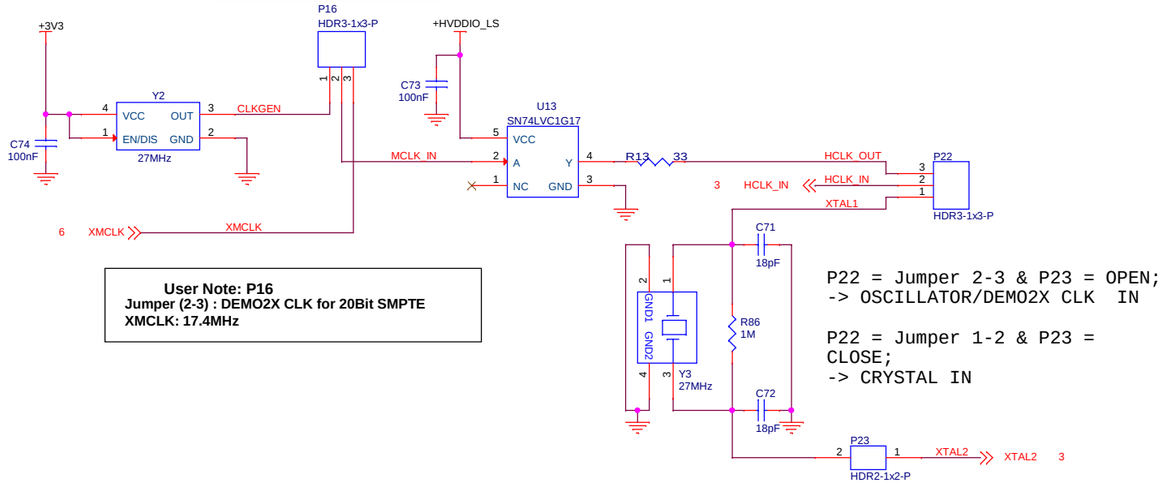
Clock/Reset/I2C Interface

CLOCK CIRCUIT

User Note: P16
Jumper (1-2) : OSC CLK
Jumper (2-3) : DEMO2X CLK

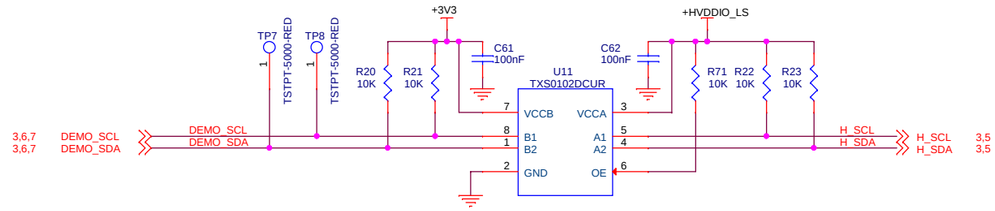


P22 = Jumper 2-3 & P23 = OPEN;
-> OSCILLATOR/DEMO2X CLK IN

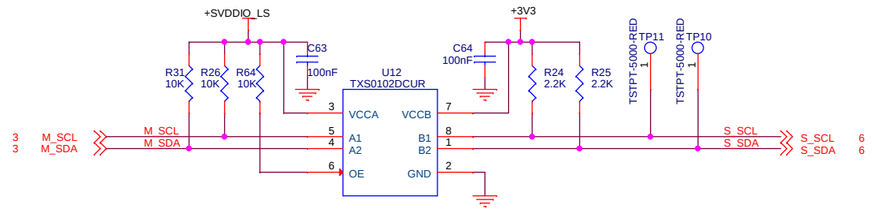
P22 = Jumper 1-2 & P23 = CLOSE;
-> CRYSTAL IN

User Note: P16
Jumper (2-3) : DEMO2X CLK for 20Bit SMPTE
XMCLK: 17.4MHz

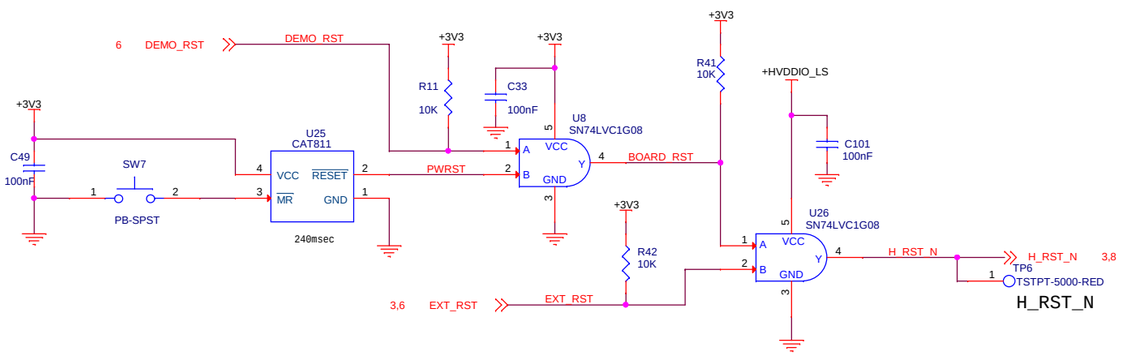
Host I2C BUFFER



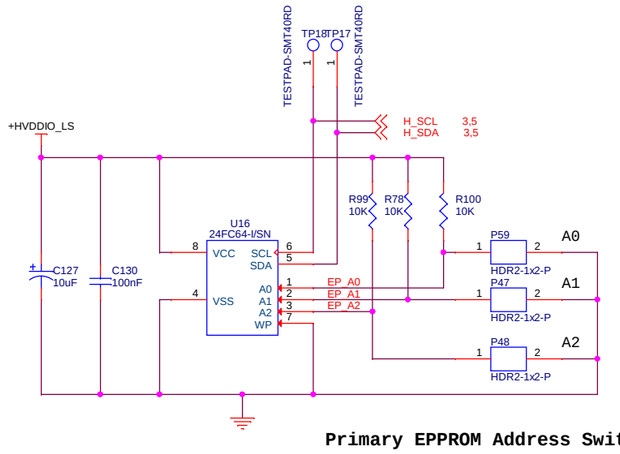
Sensor I2C BUFFER



RESET CIRCUIT



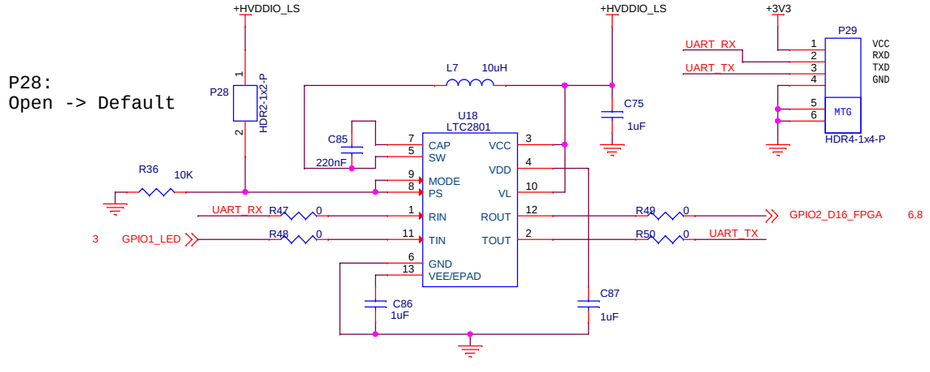
H_RST_N



Primary EPPROM Address Switch Settings:

```
A2=HIGH, A1=LOW,  A0=HIGH; Address => 0xAA (default)
A2=LOW,  A1=LOW,  A0=HIGH; Address => 0xA2
A2=LOW,  A1=HIGH, A0=HIGH; Address => 0xA6
A2=HIGH, A1=HIGH, A0=HIGH; Address => 0xAE
```

P28:
Open -> Default



4,6,7	+5V0	+5V0
3,4	+VDD_REG	+VDD_REG
3,4	+SVDDIO	+SVDDIO
3,4	+HVDDIO	+HVDDIO
3,4,6,7	+3V3	+3V3
4,6	+SVDDIO_LS	+SVDDIO_LS
3,4,6,7	+HVDDIO_LS	+HVDDIO_LS
3,4	+OTPM_VCC	+OTPM_VCC
4,8	+VCCIO	+VCCIO
4,7,8	+3V3_HVCCIO	+3V3_HVCCIO
4,8	+1V2_VCCINT	+1V2_VCCINT
4,8	+2V5_VCCA	+2V5_VCCA

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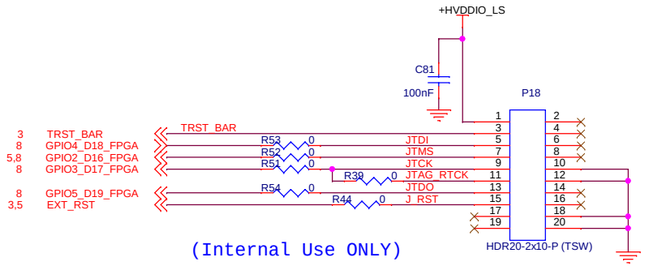
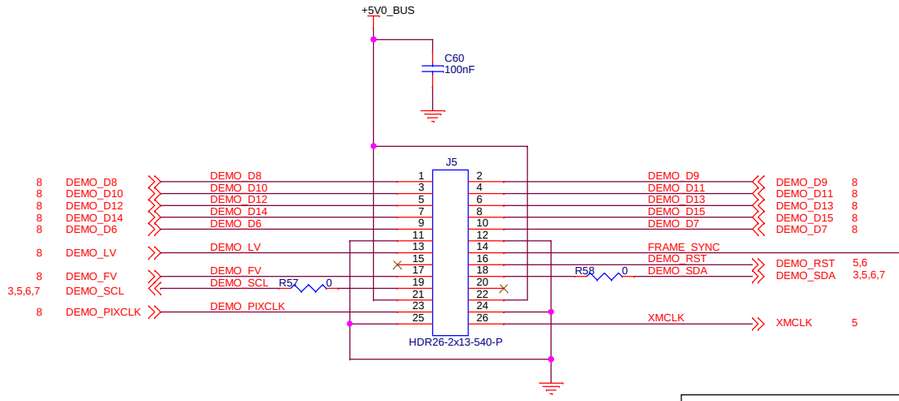
External Interface

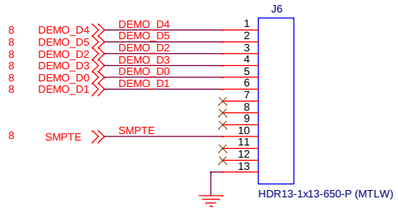


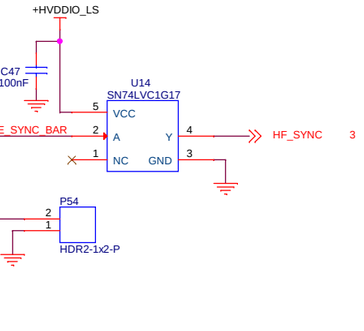
(Internal Use ONLY)

Demo2X I/F



Demo2X I/F

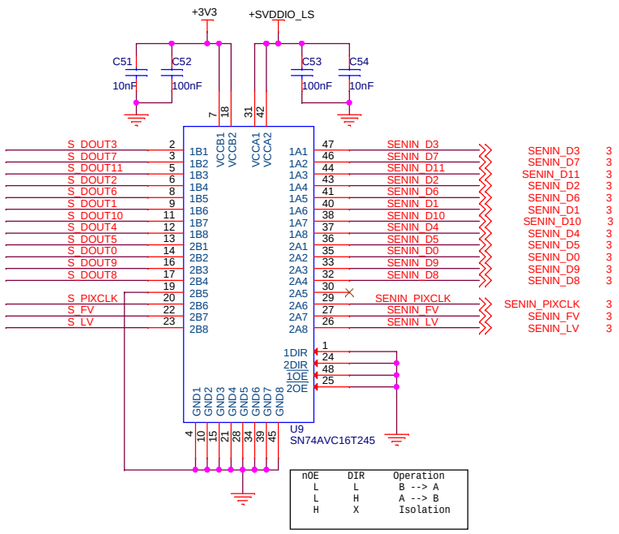




DEMO2X access to SYNC signal (Default):
Close P33 --> Pin 1-2
Open P54

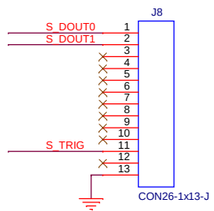
EXT access to SYNC signal:
Open P33
Input Signal P54 --> Pin 2
Input signal Voltage => 2.8V ~3.3V

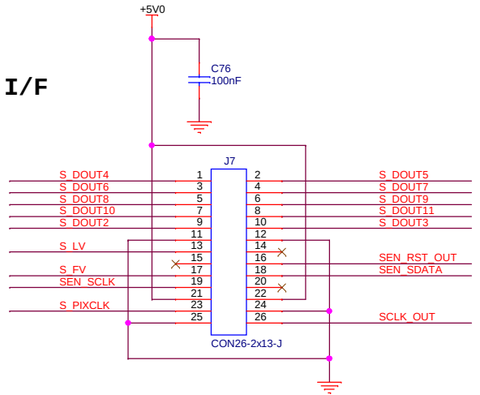
Parallel Data Level Shifter (HeadBoard -> AP0101 board)

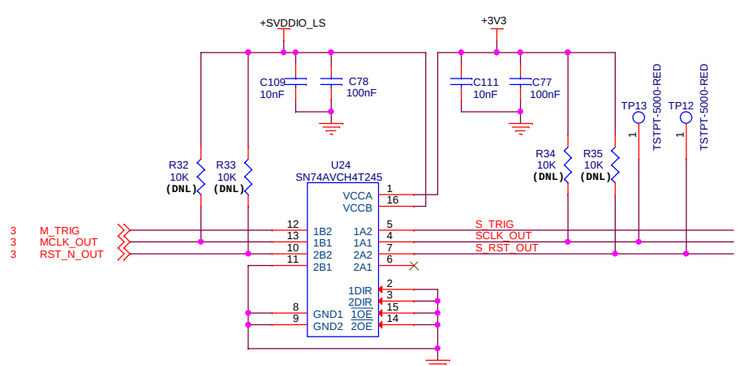


nOE	DIR	Operation
L	L	B --> A
L	H	A --> B
H	X	Isolation

Headboard I/F

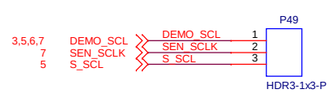






P51
Pins 2 - 3 --- DEMO2X Reset
Pins 1 - 2 --- AP0101 Reset (default)

P50
Pins 1 - 2 --- DEMO2X serial control
Pins 2 - 3 --- AP0101 serial control (default)



P49
Pins 1 - 2 --- DEMO2X serial control
Pins 2 - 3 --- AP0101 serial control (default)

Aptina IMAGING

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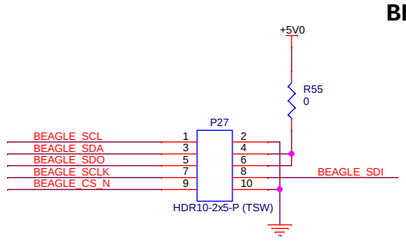
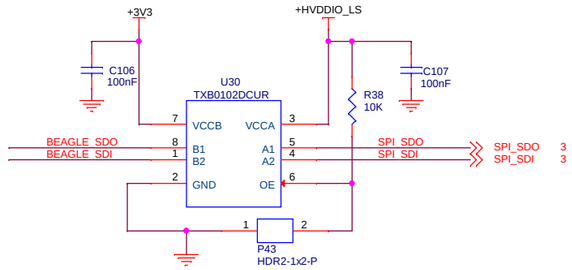
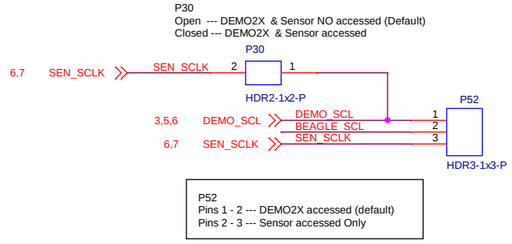
BEAGLE/FPGA EXT I/F

BEAGLE I/F



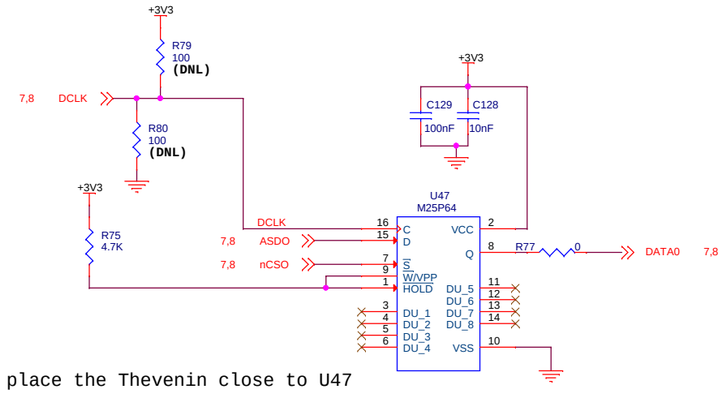




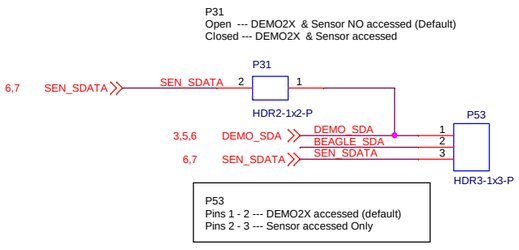
Beagle access to SPI Bus:
Open P44
Open P43

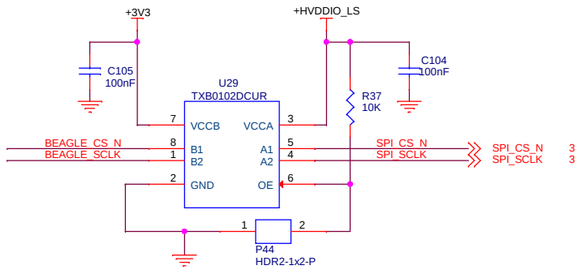
Beagle no access to SPI Bus (Default):
Close P44 --> Pin 1-2
Close P43 --> Pin 1-2

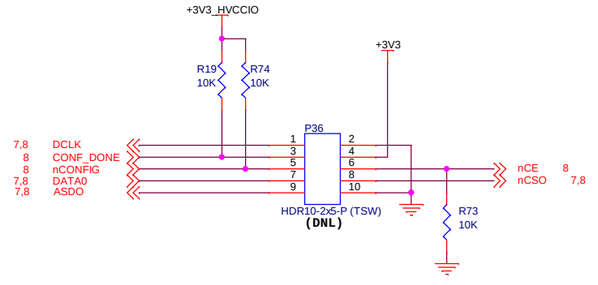
FPGA Memory I/F



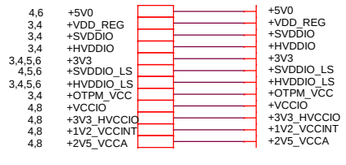
place the Thevenin close to U47







Beagle Serial configuration			
Header	Pin condition	Signal connection	Remark
P52/P53	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Remove R58/R57 DEMO2X master remove
P52/P53	Pin 2-3	BEAGLE_Serial => SEN_Serial	Beagle master control Sensor, no control on AP0101
P52/P53 & P49/P50	Pin 1-2 OPEN for P49/P50	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, Open P50/P49 AP0101 master remove to Sensor
P52/P53 & P30/P31	Pin 1-2 Close for P30/P31	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, AP0101 serial to Sensor still connected



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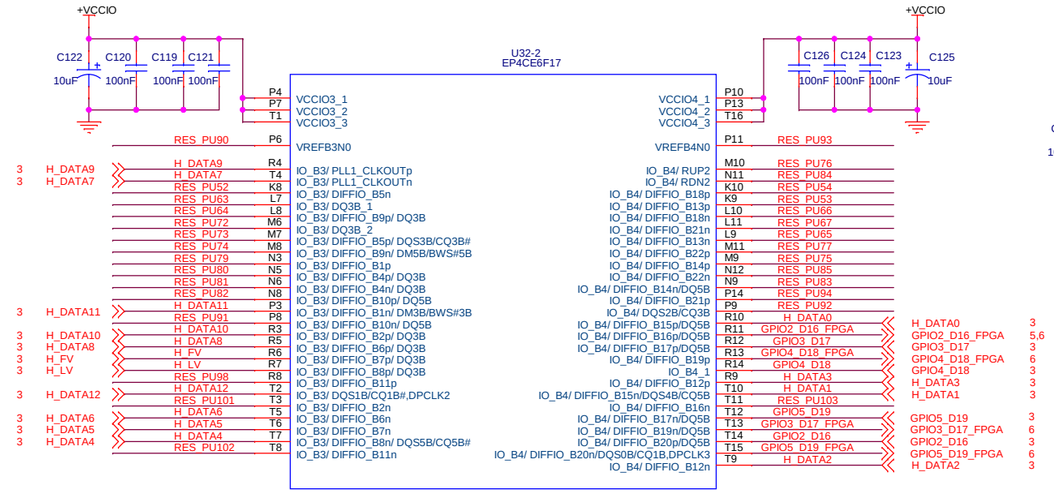
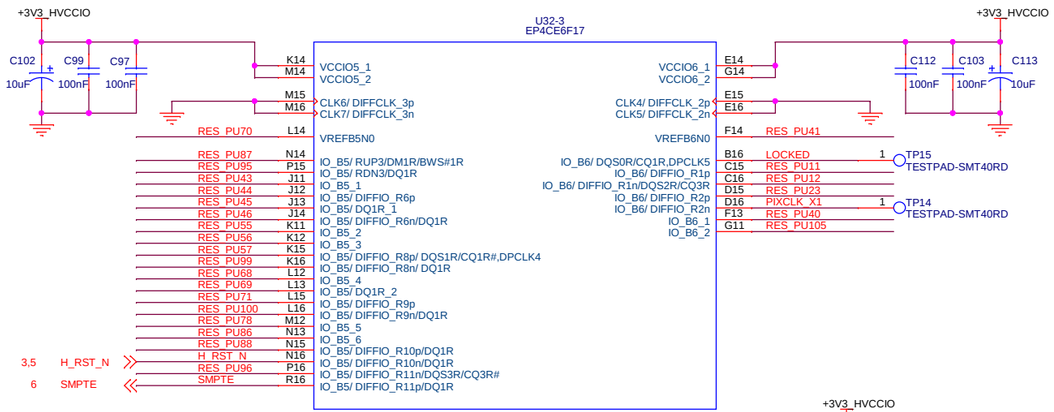
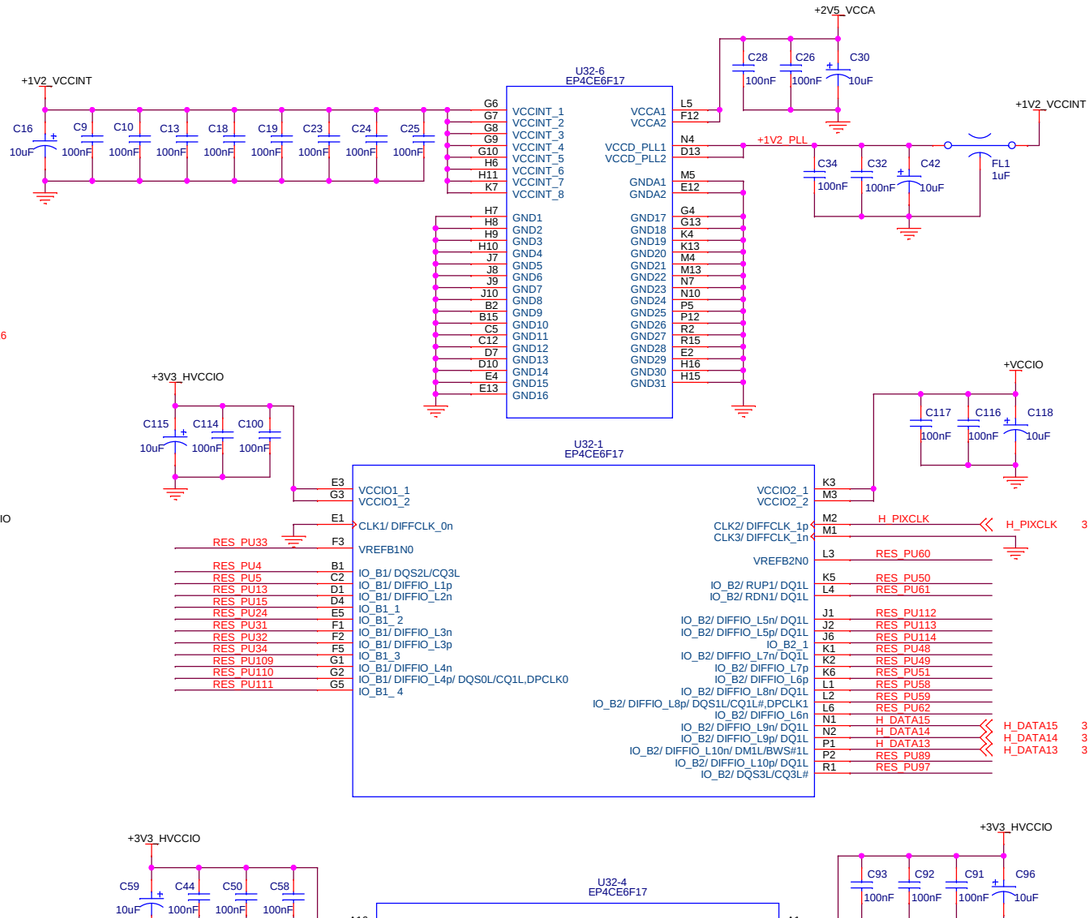
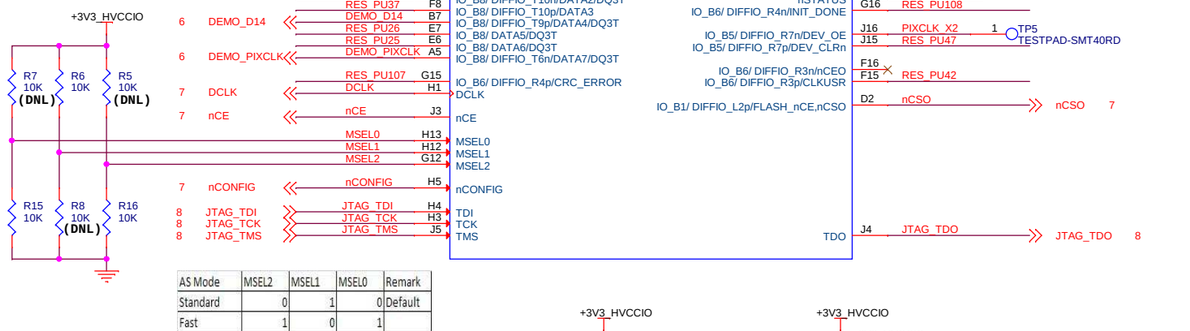
FPGA Interface

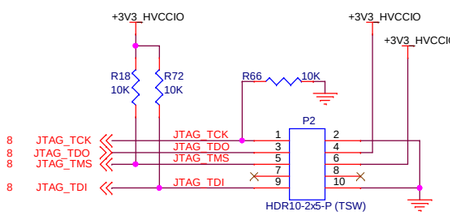


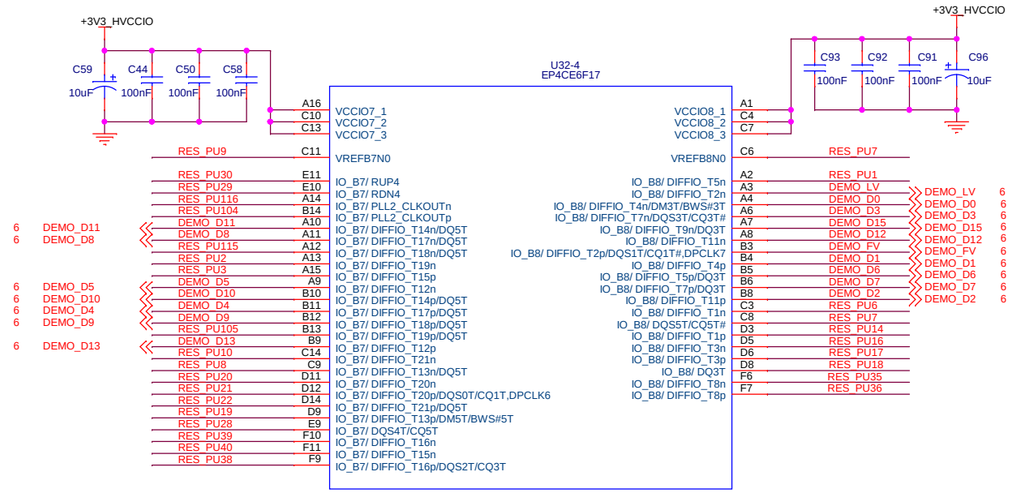


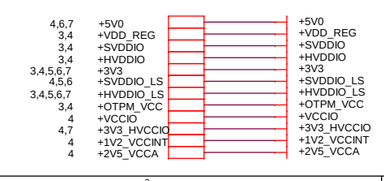




AS Mode	MSEL2	MSEL1	MSEL0	Remark
Standard	0	1	0	Default
Fast	1	0	1	







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Configuration Setting

Beagle Serial configuration			
Header	Pin condition	Signal connection	Remark
P50/P49	Pin 2-3	AP0100_Serial => SEN_Serial	AP0101 master control Sensor
P50/P49	Pin 2-3	AP0100_Serial => SEN_Serial	AP0101 master control Sensor
P52/P53	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Remove R58/R57 DEMO2X master
P52/P53	Pin 2-3	BEAGLE_Serial => SEN_Serial	Beagle master control Sensor, no control on AP0101, Open
P52/P53 & P49/P50	Pin 1-2 OPEN for P49/P50	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Open P50/P49 AP0101 master remove to Sensor, Open P30/P31
P52/P53 & P30/P31	Pin 1-2 Close for P30/P31	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, AP0101 serial to Sensor still connected
P49/P50,P52/P53 & P30/P31	Pin 1-2 Close for P30/P31 OPEN for P49/P50	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, Open P50/P49 AP0100 master remove to Sensor
Auto-configuration			
Header	Pin condition	Signal Condition	Remark
P43/P44	P44 = Short 1-2/P43 = Short 1-2	Disable U30/U29	Beagle no access to SPI Bus
P5/P45	P5 = Short 1-2/P45 = Open	Host Mode (SPI_SDI = GND)	SPI_SDI Table:
	P5 = Open/P45 = Open	Flash Mode (SPI_SDI = Flash/EEPROM Data)	SPI_SDI => High Impedance (Auto-config)
	P5 = Short 1-2/P45 = Short 1-2	Auto-Configuration (SPI_SDI = High Impedance)	SPI_SDI => Data (Flash Mode)
	P5 = Open/P45 = Open	Host/Flash/Auto-Config	SPI_SDI => Serial Control Mode type
P43/P44	P43/P44 = Short 1-2	SP1_SDO/SDI/SCLK/CS_N	Disable Beagle SPI access

4,6,7	+5V0	+5V0
3,4	+VDD_REG	+VDD_REG
3,4	+SVDDIO	+SVDDIO
3,4	+HVDDIO	+HVDDIO
3,4,5,6,7	+3V3	+3V3
4,5,6	+SVDDIO_LS	+SVDDIO_LS
3,4,5,6,7	+HVDDIO_LS	+HVDDIO_LS
3,4	+OTPM_VCC	+OTPM_VCC
4,8	+VCCIO	+VCCIO
4,7,8	+3V3_HVCCIO	+3V3_HVCCIO
4,8	+1V2_VCCINT	+1V2_VCCINT
4,8	+2V5_VCCA	+2V5_VCCA

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